D2P Technology Analysis – Reviewer #1

Pat. No.: US 7,184,723
"Systems and Methods for Vector Power Amplification"
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OVERVIEW

The stated goal here is to provide a novel method which gives both linearity and high efficiency in an integratable power amplifier solution. The method proposes to split the incoming signal, or have multiple signals provided, amplify them using constant envelope power amplifiers and then sum the outputs with a novel combining method. Constant envelope amplifiers can be made extremely efficient and do not distort the signal as long as the constant envelope is maintained.

The big issues here are novelty and feasibility. The power splitting, constant envelope amplification, and combining to produce a time varying output goes back to Chireix in 1935 [1]. Others have proposed variations on this theme [1]. The combining technique is also not new as paralleling transistor outputs is used in every current-summing digital-to-analog converter, power supplies, and logic gates [3]. So separately these techniques are not new and the next major issue is if these ideas actually work to provide efficiency and linearity when used together. This second issue must be answered with a negative because the proposed combining technique would only allow the efficiency and linearity claimed if transistors were ideal current sources without parasitics. Real world device parasitics cause the proposed combining scheme to reduce both efficiency and linearity.

A realization of this patent for independent examination and comparison to the current state-of-the-art, or simulations with transistor tolerances and temperature variations should be enough to highlight all of the real issues with this methodology.

This reviewer, who has had significant experience with combining networks such as those described in this patent as well as those which provide isolation, believes the inventors to be ignorant of the real issues in combining networks.

In short, this proposed combining technique would only work if transistors are ideal current sources, which they are not. In regions (low frequency, low power) where transistors behave close to ideal current sources this summing technique is already in use. All of the distortion and efficiency claims are negated by the fact that the combining method described creates load impedance changes which reduce efficiency and it creates non-constant envelope waveforms that increase distortion.

This means that any attempt to use this idea for a commercial product would require a much higher speed (and so more expensive) integrated circuit process to reduce the transistor parasitics. Any real design improvement in power amplifier efficiency and linearity will show an awareness of transistor parasitics and nonlinearities.

Some of the information in this patent, such as the background/prior art section is woefully inadequate. For example, Class D is a switching amplifier with high efficiency and high linearity.

The problem with Class D is that transistor parasitics limit the power/bandwidth capability. Class D is highly integratable.

CLAIMS

The independent claims of this patent are 1 and 41.

Claims 1 and 41 as read by this researcher, covers the original Chireix amplifier with no distinguishing added features.

The single summing node restriction in Claims 1 and 41, while definitely minimizing the size of the combining network, introduces many problems which are not addressed in the patent.

The single summing node aspect of the claim makes no sense to RF designers because the Chireix amplifier could be realized as a load between two devices or a load connected to ground and then both devices (one device having a 180 degree phase shift inserted). With regard to efficiency, the single summing node suffers because if the net drive signal is to be zero then current sourced from one amplifier must be sunk by a second amplifier. This results in a current drain on the supply with no power transfer to the load and hence reduces efficiency. The original Chireix used a load between two devices (similar to an H-bridge motor driver) and so required no current drain if the signal was in-phase on both devices.

In a sense Claim 1 can be realized by an IQ ADC integrated circuit and a high-speed current summing DAC (available from TI (GC2011), Analog Devices (DAC16), Broadcom (BCM3040), or Agilent and used in telecom or arbitrary waveform generators). These devices are not known for their efficiency even though they are digital switching devices. Any real examination of their accuracy (linearity) shows a great deal of attention to transistor parasitics, nonlinearities, variations, and calibration. The constant envelope criteria from Claim 1 is not maintained in most current switching DACs, but would hold if the DACs were realized as complementary current sources shown in Figure 51 with no “off” state.

SUMMARY

While not significant legally, the patent description and summary shows the intent of the patent to improve linearity, efficiency, and monolithic integration. This summary can be easily dismissed as each of its claims proves false. The initial Chireix amplifier article clearly defines a plurality of constant envelope amplifiers being combined to increase system efficiency. This article was published in 1935 [1]. The second statement of the summary is that the combining technique is novel and not taught or found in the literature or related art. Even a cursory glance at digital design literature will show digital-to-analog converters using many transistors with their collectors (or drains) connected to a common junction [2,3]. Glances at audio amplifier literature will show Figures 38,42, and 51 as examples of complementary and non-complementary amplifier output stages [2,3].

While reference [3] goes into detail regarding transistor models which allow an engineer to assess the impact of device nonlinearities on a combiner such as a single summing junction, this patent

completely ignores the issue. The most obvious factor here is that summing various constant envelope signals with varying phase at a single junction will produce a non-constant envelope. Therefore all of the previously assumed constant envelope amplifiers now have their output stage operating at a non-constant envelope. The time variation of this envelope will cause intermodulation distortion between the various amplifiers, as well as limit the efficiency of the various amplifiers because the load impedance to each amplifier will now be varying with time. As well, the varying envelope will create voltage variations which will introduce distortion through the nonlinear capacitance and output resistance of each device. All of these factors will be seen in a detailed simulation using accurate transistor models which are readily available today. Currently, as well as in the past, these issues are solved by providing combining networks with isolation between the various amplifiers – a solution this patent explicitly claims to avoid using.

In conclusion, this patent fails to be convincing on several points:

- There is no explanation of how this is an advance on prior art such as the Chireix method;
- There is no explanation of how this method improves on or solves the known problems in the Chireix method;
- There is no explanation of how transistor parasitic capacitances and nonlinear IV characteristics limit the bandwidth, efficiency, linearity and realization of this method;
- There is no explanation of the impact of the proposed non-isolating signal combining network on the bandwidth, linearity and efficiency of the system.
- There is no comparison of the proposed non-isolating signal combining network to isolating approaches in terms of size, insertion loss, bandwidth, and effect on system linearity.

REFERENCES

[1] Cripps, Advanced Techniques in RF Power Amplifier Design, Artech House, 2002.
[2] Huijsing, van der Plassche, and Sansen, Analog Circuit Design, Kluwer, 1993.
[3] Geiger, Allen, and Strader, VLSI Design Techniques for Analog and Digital Circuits, McGraw Hill, 1990.