NO: 433132US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

_____

BEFORE THE PATENT TRIAL AND APPEAL BOARD

_____

DR. MICHAEL FARMWALD
and
RPX CORPORATION.
Petitioners,

v.

PARKERVISION, INC.,
Patent Owner.

_____

Case IPR2014-_____
Patent U.S. 7,496,342

_____

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 7,496,342 UNDER 35 U.S.C. § 312 AND 37 C.F.R. § 42.104

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TABLE OF CONTENTS

Page

I. MANDATORY NOTICES 1

II. CERTIFICATION OF GROUNDS FOR STANDING 2

III. OVERVIEW OF CHALLENGE AND RELIEF REQUESTED 2

A. Prior Art Patents and Printed Publications 2

B. Grounds for Challenge 3

IV. OVERVIEW OF THE '342 PATENT 4

A. Background: Differential Circuits 5

B. The '342 Patent 6

C. Effective Filing Date of the Challenged Claims 11

V. CLAIM CONSTRUCTION 16

VI. LEVEL OF ORDINARY SKILL IN THE ART 22

VII. STATEMENT OF MATERIAL FACTS 22

VIII. IDENTIFICATION OF HOW THE CHALLENGED CLAIMS ARE UNPATENTABLE 28

A. Claims 18 and 23 are Anticipated by Oxner under 35 U.S.C. § 102 (b) 29

B. Claims 18, 19, 20, 21, and 23 are rendered obvious under 35 U.S.C. § 103 by the '551 patent in view of knowledge of one of ordinary skill in the art, as evidenced by Razavi, Thornton or Bult. 32

C. Claims 18, 19, 20, 21, and 23 are rendered obvious under 35 U.S.C. § 103 by Estabrook in view of knowledge of one of ordinary skill in the art, as evidenced by Razavi, Thornton or Bult. 37

IX. CONCLUSION.....44

TABLE OF AUTHORITIES

Page

Cases

In re GPAC Inc., 57 F.3d 1573 (Fed. Cir. 1995) 22
Interactive Gift Exp., Inc. v. Compuserve Inc., 256 F.3d 1323 (Fed. Cir. 2001) 22
Lockwood v. Am. Airlines, Inc., 107 F.3d 1565 (Fed. Cir. 1997)..... 11, 12, 15
Ralston Purina Co. v. Far-Mar-Co., Inc., 772 F.2d 1570 (Fed. Cir. 1985).....16
Vitronics Corp. v. Conceptronic, Inc., 90 F.3d 1576 (Fed. Cir. 1996).....21

Statutes

35 U.S.C. § 102(b) 3, 32
35 U.S.C. § 314(a) 4
37 C.F.R. § 42.100(b) 16
37 C.F.R. § 42.22 22
37 C.F.R. § 42.8(b)(4).....1

Rules

42.104 (b)(1)-(2) 2
42.104(a) 2
42.104(b)(4)-(5) 28
42.22(a)(1).....2

I. MANDATORY NOTICES

Real Parties-in-Interest: RPX Corporation and Dr. Michael Farmwald (hereinafter collectively referred to as "Petitioners").

Related Matters: The following matters would affect or be affected by a decision in this proceeding: *ParkerVision, Inc. v. Qualcomm, Inc.*, Case No. 3:11-cv-719-J-37TEM (M.D. Fla.) (hereinafter "the Qualcomm litigation").[1]

Lead and Back-Up Counsel: Petitioners provide the following designation of counsel: Lead counsel is W. Todd Baker (Reg. No. 45,265) and back-up counsel is James T. Bailey (Reg. No. 44,518).

Service Information: Pursuant to 37 C.F.R. § 42.8(b)(4), papers concerning this matter should be served on the following. Petitioners consent to electronic service.

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[1] Qualcomm is not a current client of RPX Corporation. All docket items referenced herein and included as Exhibits were retrieved from patentee's publicly available website at www.http://www.parkervision.com/public_relations/patent_litigation.php

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II. CERTIFICATION OF GROUNDS FOR STANDING

Petitioners certify pursuant to Rule 42.104(a) that the patent for which review is sought is available for *inter partes* review and that Petitioners are not barred or estopped from requesting an *inter partes* review challenging the patent claims on the grounds identified in this Petition.

III. OVERVIEW OF CHALLENGE AND RELIEF REQUESTED

Pursuant to Rules 42.22(a)(1) and 42.104 (b)(1)-(2), Petitioners challenge claims 18, 19, 20, 21, and 23 of U.S. Patent No. 7,496,342 (Ex. 1001, "the '342 patent").

A. Prior Art Patents and Printed Publications

Petitioners rely upon the following patents and printed publications, none of which was considered during the original prosecution of the '342 patent with the exception of U.S. Patent No. 6,061,551:

Exhibit 1004 – E. Oxner, Siliconix Application Note AN72-1 "FETs in Balanced Mixers," 1979. ("Oxner");

Exhibit 1005 – U.S. Patent No. 6,061,551 ("the '551 patent").

Exhibit 1006 – Polly Estabrook, "The direct conversion receiver: Analysis and design of the front-end components," (Ph.D diss., Stanford University, 1989). ("Estabrook");

Exhibit 1007 – B. Razavi, "Principles of Data Conversion System Design," IEEE Press 1995. ("Razavi");

Exhibit 1008 – Richard D. Thornton *et al.*, "Multistage Transistor Circuits: Semiconductor Electronics Education Committee, Volume 5," *John Wiley & Sons Inc.* 1965, pp. 201-07. ("Thornton"); and

Exhibit 1009 – Klaas Bult and Hans Wallinga, "A CMOS Four-Quandrant Analog Multiplier," *IEEE Journal of Solid-State Circuits*, Vol. SC-21, No. 3, June 1986, 430-35. ("Bult").

Oxner, the '551 patent[2], Estabrook, Razavi, Thornton, and Bult are available as 35 U.S.C. § 102(b) art against the challenged claims of the '342 patent.

B. Grounds for Challenge

Petitioners request cancelation of the challenged claims under the following statutory grounds:

A. Claims 18 and 23 are anticipated under 35 U.S.C. § 102(b) by Oxner.

[2] As established below in Section IV.C, for all of the challenged claims, the effective filing date of the '342 patent is no earlier than May 16, 2001. Thus, the '551 patent constitutes 35 U.S.C. §102(b) prior art and can be applied in an obviousness type of patentability challenge pursuant to 35 USC §103(c).

B. Claims 18, 19, 20, 21, and 23 are rendered obvious under 35 U.S.C. § 103 by US Patent No. 6,061,551 in view of knowledge of one of ordinary skill in the art, as evidenced by Razavi, Thornton, or Bult.

C. Claims 18, 19, 20, 21, and 23 are rendered obvious under 35 U.S.C. § 103 by Estabrook in view of knowledge of one of ordinary skill in the art, as evidenced by Razavi, Thornton, or Bult.

Section VIII below demonstrates, for each of the statutory grounds, that there is a reasonable likelihood that Petitioners will prevail with respect to at least one of the challenged claims. *See* 35 U.S.C. § 314(a).

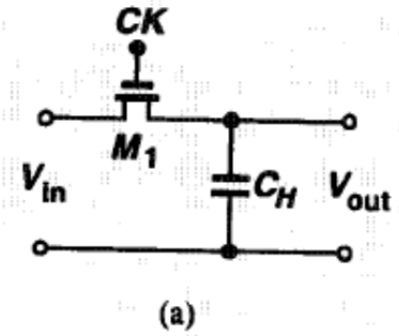
IV. OVERVIEW OF THE '342 PATENT

The '342 patent generally relates to translating the frequency of a signal, either down-conversion of a carrier frequency to a lower frequency signal, which could be an intermediate frequency signal (IF) or directly to baseband frequency, or up-conversion of a signal to a higher frequency. The claims challenged in this petition, however, relate solely to down-conversion. In particular, the challenged claims all relate to methods of down-conversion using differential circuits, which were well known to those of skill in the art. The sub-sections below include a general discussion of differential circuits, the particular differential embodiments described in the specification of the '342 patent, and the earliest applicable priority date for the challenged claims.

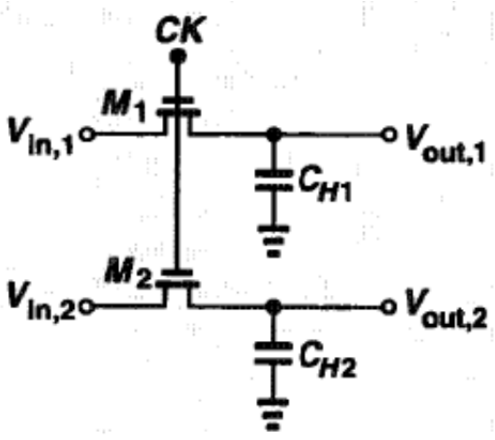
A. Background: Differential Circuits

Differential circuits and their benefits were well-known to those of skill in the art long before the alleged invention of the '342. (Ex. 1007 25-26; Ex. 1008 201-07; Ex. 1009 430-31; Ex. 1002 §6.)

Differential circuits were known to be designed by simply taking a single-ended circuit, *i.e.* a circuit with only one input and one output, and mirroring it about a line of symmetry to create a circuit with two inputs and two outputs. For example, one could start with a simple sampling circuit as shown in Figure 2.5(a) of Razavi, reproduced below. (Ex. 1007 14.)



The differential version of this circuit is then shown in Figure 2.16(b). (*Id.* 26.)



"In this topology, $V_{in,1}$ and $V_{in,2}$ are differential inputs (i.e., they vary by the same amount but in opposite directions) and $V_{out,1}$ and $V_{out,2}$ are differential outputs (i.e., their *difference* is sensed by the following circuit)." (*Id.* 25-26, emphasis in original.) While there are multiple ways to generate differential inputs, one simple and well-known method is to simply invert a first input to get the second input. (Ex. 1002 §6.)

B. The '342 Patent

The '342 patent describes performing frequency translation – either down-conversion or up-conversion – using a "universal frequency translation" (UFT) module. (Ex. 1001 6:25-33.) While the UFT module is described as "a very powerful and flexible device," it is generally simply a switch, as depicted in FIG. 1B. (*Id.* 6:30-62.)

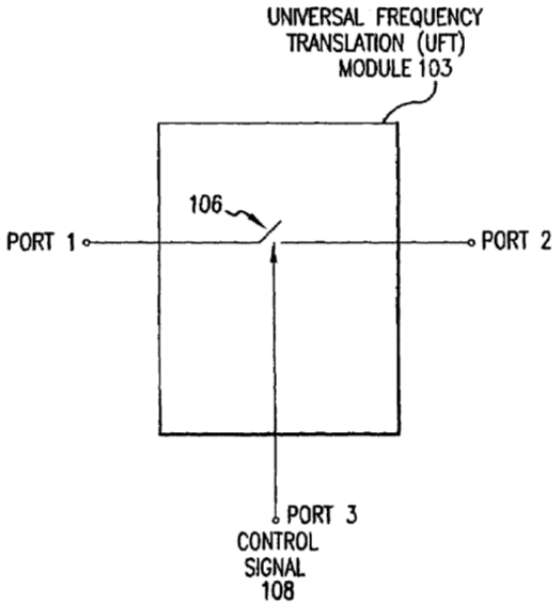


FIG. 1B

The specification states that virtually any type of switch may be utilized as a UFT module. (*Id.* 6:34-58, FIGS. 1A-B, 2.)

The only challenged independent claim, claim 18, describes a method of down-conversion using a particular set of circuitry components including a first and second switching device, a first and second capacitor and first and second impedance devices. (*Id.* 52:37-57.) Embodiments containing these paired components are first discussed in section 3.1.2 of the '342 patent, titled "Receiver Embodiments having two Aliasing Modules." (*Id.* 17:63-21:59.)

In that section, the operation of FIG. 16A is described in detail. As can be seen, FIG. 16A, reproduced below, consists of two mirrored aliasing modules, 1632 and 1634 (each containing a switch and a capacitor) and two impedance devices, 1616 and 1618. (*Id.* FIG. 16A; 18:13-22)

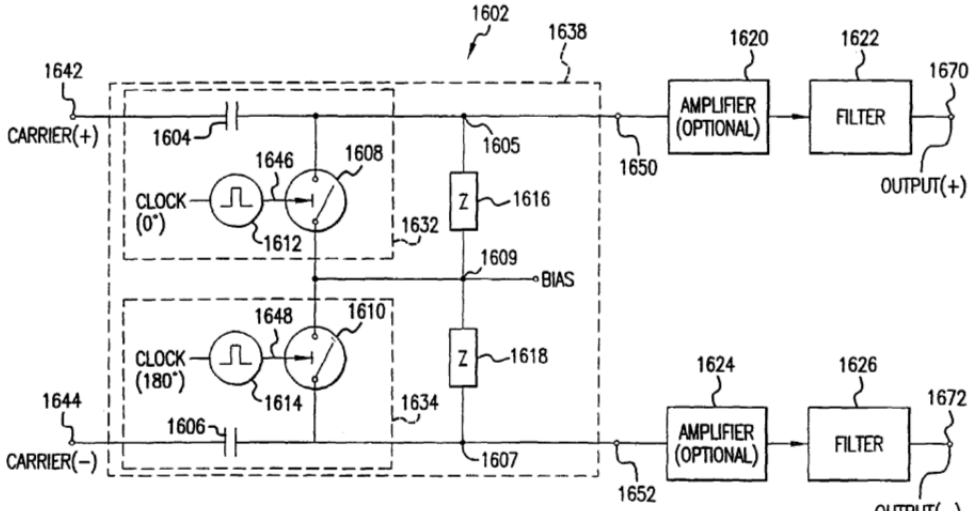
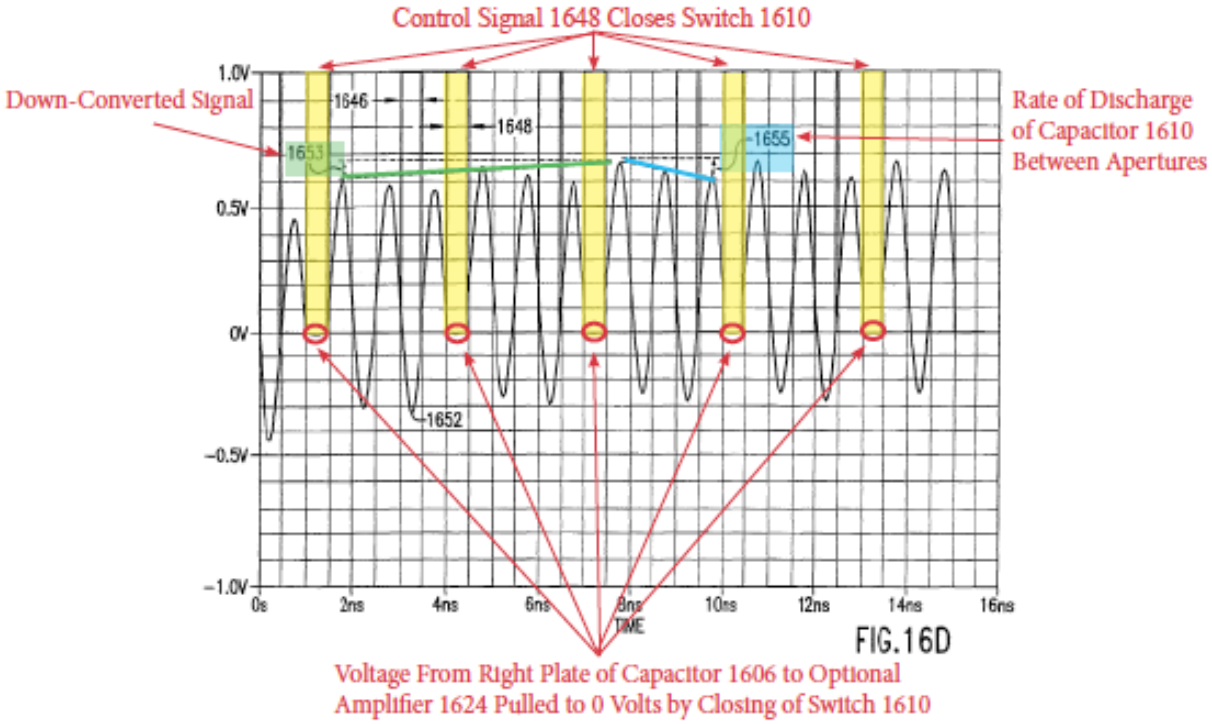


FIG.16A

In this embodiment, the capacitors are placed upstream of the switches. (*Id.* FIG. 16A.) The operation of the two mirrored aliasing modules of FIG. 16A are described with reference to FIGS. 16C-D. (*Id.* 18:42-19:8.)

For example, the output 1652 from the lower half of the circuit of FIG. 16A is shown in FIG. 16D, annotated below for ease of explanation.



As shown in FIG. 16D, each time the control signal 1648 goes on, it closes switch 1610 pulling the node extending from the left side of the capacitor 1606 to the optional amplifier 1624 down to zero volts. During this "aperture," charge accumulates on the left-hand plate of capacitor 1606. When switch 1610 is open, capacitor 1606 acts as an AC-coupling capacitor, effectively allowing the RF input signal to pass through it. In the specification this phenomenon is described as the

carrier signal "riding on top of the down-converted signal." (Ex. 1001 20:53-55.) As described in the specification, between apertures while the AC-coupled RF signal is being passed through the capacitor some of the charge accumulated during the aperture period is discharged resulting in the successive peaks caused by the RF signal to decrease each cycle of the RF signal. Accordingly, "[s]lope 1655 represents the rate of discharge of capacitor 1606 between apertures." (*Id.* 19:3-5.)

The specification states that "[i]n FIG. 16D, slope 1653 represents the down-converted signal." (*Id*. 19:2-3.) As can be seen from FIG.16D, the down-converted signal 1653 is effectively the interpolation between peak voltages resulting from each charging cycle. As described in the specification, in this embodiment, the RF carrier signal can be removed from the down-converted signal either by the optional filter 1626, the optional amplifier 1642, or a combination of the two. (Ex. 1001 19:5-8; 20:13-17.)

The '342 specification also includes another differential embodiment, in which the capacitors are situated downstream of the switches, as shown in FIG. 16H.

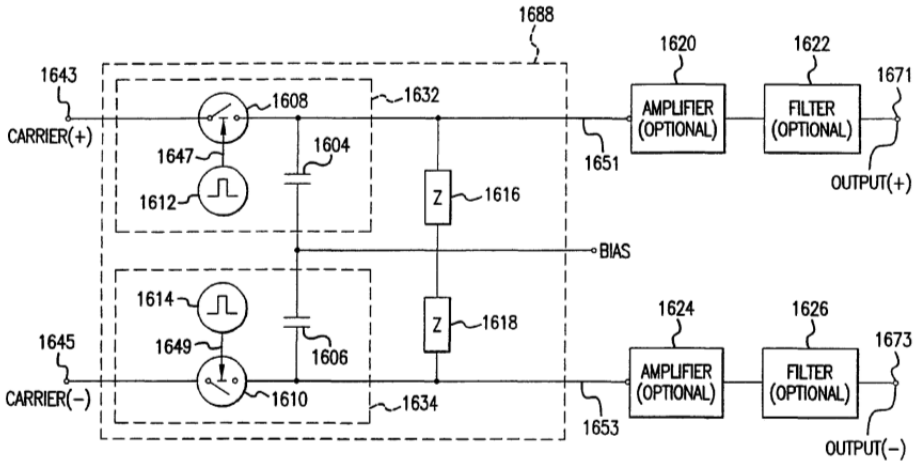


FIG.16H

The specification notes that the embodiment of FIG. 16H "operates similarly" to the embodiment of FIG. 16A "except that the carrier signal is removed from the down converted signal by capacitors 1604 and 1606 during down-conversion." (*Id.* 20:33-39.) The output of the two mirrored aliasing modules of FIG. 16H is shown in FIGS. 16J-L. (*Id.* 20:49-50.)

For example, the output 1651 from the upper half of the circuit of FIG. 16H is shown in FIG. 16J, annotated below for ease of explanation.

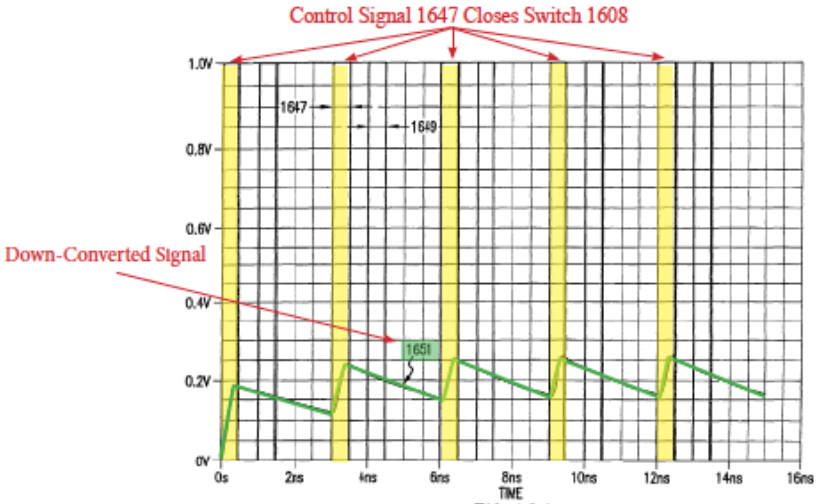


FIG.16J

Each time control signal 1647 closes switch 1608, the carrier signal is connected to the capacitor 1604 resulting in charging of that capacitor. When the switch is open, capacitor 1604 discharges through the remainder of the circuit. As noted above, the carrier signal has been removed.

C. Effective Filing Date of the Challenged Claims

The '342 patent issued from a division of a continuation-in-part application (No. 09/855,851, "the '851 application") filed on May 16, 2001 and also claims priority to three different provisional applications. (Ex. 1001 Cover.) In the Qualcomm litigation, patentee asserted that the priority date for all of the challenged claims of the '342 patent was "no later than" the May 16, 2001 filing of the '851 continuation-in-part application. (Ex. 1010: D.I. 152-1 at 4; *see also id*. at 2 (identifying the "Asserted Claims").) As discussed below, for all of the challenged claims the priority date is no earlier than May 16, 2001.

"Entitlement to a filing date does not extend to subject matter which is not disclosed, but would be obvious over what is expressly disclosed. It extends only to that which is disclosed." *Lockwood v. Am. Airlines, Inc.*, 107 F.3d 1565, 1571-72 (Fed. Cir. 1997). . "The question is not whether a claimed invention is an obvious variant of that which is disclosed in the specification. Rather, a prior application itself must describe an invention, and do so in sufficient detail that one skilled in the art can clearly conclude that the inventor invented the claimed

invention as of the filing date sought." *Id*. at 1572. "One shows that one is 'in possession' of *the invention* by describing *the invention,* with all its claimed limitations, not that which makes it obvious." *Id.* (emphasis in original). The applications filed prior to May 16, 2001 do not satisfy this standard.

As noted above, challenged independent claim 18 is limited to a method of differential down-conversion using particular circuit elements, including first and second switching devices, first and second capacitors and first and second impedance devices. (Ex. 1001 52:37-57.) This invention is not disclosed in Application No. 09/550,644 ("the '644 application")[3]. The materials describing differential embodiments in the '342 specification discussed above – FIGS. 16A, 16H and section titled "Receiver Embodiments having two Aliasing Modules" – were new matter added in the '851 application. (*Cf*. Ex. 1001, 1011.)

While the material disclosed in the '644 application, which is highly duplicative of the material in the '551 patent discussed below, would render the "invention" of the '342 patent obvious, it does not disclose the limitations of claim 18. The '644 application describes certain differential embodiments none of them

[3] The '644 application ultimately issued as U.S. Patent No. 7,515,896. (Ex. 1011.) For ease of reference, citations to the '644 written description will be made to the '896 patent and to the originally filed claims of the '644 application, Exhibit 1022, as necessary.

include all of the limitations of claim 18. For example, many of the differential or "pseudo differential" embodiments of the '644 application use only one switch, instead of the two required by claim 18. (Ex. 1011 FIGS. 44A-E, 76A-E, 101, 218A, 233, 262.) Other embodiments describe use of two switches, but only one capacitor instead of the two required by claim 18. (Ex. 1011 FIGS. 99, 100, 102, 242, 261.) Still other embodiments show at least two switches and two capacitors, but lack the required step of inverting an information signal. (Ex. 10011 FIGS. 197, 213, 218B.) FIG. 144 of the '644 application could be interpreted as having two switches, two capacitors and two impedance devices within the respective RF/Switch Integrators 14408 and 14410 as shown, for example, in FIG. 137. However, this embodiment still does not disclose the invention of claim 18 of the '342 patent. First, FIG. 144 does not disclose receiving an information signal and then inverting it. Instead, Figure 144 would have been understood by one of skill in the art to depict use of a dipole antenna, which receives balanced signals that are inverted versions of one another, but does not receive a signal and then invert it as required by claim 18. (Ex. 1011 FIG. 144, *see also* FIGS. 44B, 76B, 69:16-19, 124:21-24; Ex. 1002 §6.) Second, FIG. 144 is described as having a "theory of operation [that] is similar to the non-differential receiver of FIG. 135." (Ex. 1011 194:32-36.) The theory of operation of FIG. 135 is described as a sample and hold strategy. (*Id.* 192:36-43 ("The RF Switch/Integrator 13506 samples the RF signal

13606 . . . and allows the Integrator to hold the last RF signal sample 13606 until the next cycle of the Waveform Generator 13508 output.").) Systems that intend to hold a voltage between samples are expressly distinguished as being different than the invention of the '342 patent. (Ex. 1001 37:67-38:10.)

Original claims 12, 24 and 35 of the '644 application are method claims that describe performing certain operations on an "inverted" carrier signal. (Ex. 1022.) However, these claims fail to recite particular circuit elements, including first and second switching devices, first and second capacitors and first and second impedance devices. (*Id*.)

Accordingly, the '644 application does not provide written description support for claim 18 of the '342 patent. *See Lockwood*, 107 F.3d at 1571-72.

Provisional applications 60/204,796 and 60/213,363 also do not describe the invention claimed in any of the challenged claims of the '342 patent and therefore cannot support an earlier filing date. Neither discloses differential down-converters at all. (Ex. 1012; Ex. 1013.)

Provisional application 60/272,043 ("the '043 provisional") describes the structures recited in claim 18 of the '342 patent as shown in FIG. 19A, reproduced below, but does not describe the invention of claim 18 because it does not describe the step of inverting an information signal. (Ex. 1014.)

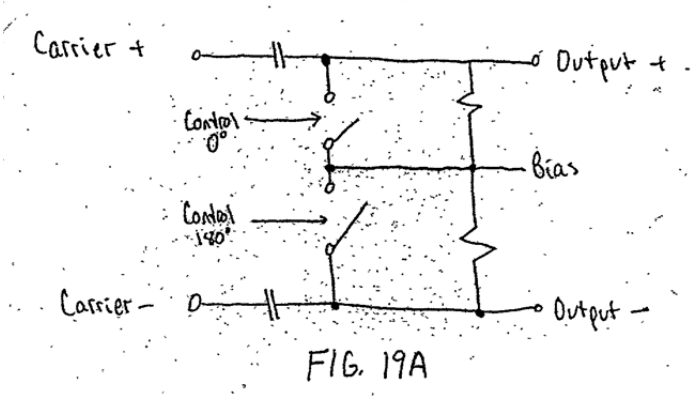


FIG. 19A

There is no discussion of FIG. 19A in the '043 provisional. (Ex. 1014) As noted in the '342 specification, inverting an information signal is only one possible way of creating an inverted information signal. (Ex. 1001 18:56-58 ("Input signal 1644 is generated in some embodiments of the invention by inverting signal 1642.").) While the step of inverting the carrier+ signal to create the carrier- signal in FIG. 19A above would have been obvious, it is not disclosed and the '043 provisional cannot support an earlier filing date for the challenged claims of the '342 patent.[4] *See Lockwood*, 107 F.3d at 1571-72.

[4] In addition, while the discharge range of 6-50% claimed in dependent claim 19 is disclosed in the '043 provisional (Ex. 1014 ¶36), the first support for the narrower ranges of dependent claims 20 and 21 is the claims themselves in the '851 continuation-in-part application (Ex. 1015), providing another reason why these claims are entitled to a priority no earlier than May 16, 2001. *See Eiselstein v. Frank*, 52 F.3d 1035, 1040 (Fed. Cir. 1995) (holding that a grandparent application

Accordingly, the earliest filing date to which any of the challenged claims is entitled is the May 16, 2001 filing date of the '851 continuation-in-part application.

V. CLAIM CONSTRUCTION

The claim terms are presumed to take on their ordinary and customary meaning. This Petition shows that the challenged claims of the '342 patent are unpatentable when the challenged claims are given their broadest reasonable interpretation in light of the specification. *See* 37 C.F.R. § 42.100(b).

The broadest reasonable interpretation in light of the specification of the claim elements, in the order they appear, is discussed below:

Electrically coupling: The parties in the Qualcomm litigation agreed to a construction of "electrically coupling" to mean "indirectly or directly connecting such that an electric signal can flow between the coupled points." (Ex. 1016: D.I. 110-1.) This is consistent with the specification, which states that "electrically coupled" does not require "physically coupled," and there can be intervening

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describing an alloy containing 45-55% nickel, did not adequately disclose the claimed range of "about 50 to about 60%" nickel content); *see also Ralston Purina Co. v. Far-Mar-Co., Inc.*, 772 F.2d 1570, 1575 (Fed. Cir. 1985) (holding that adequate disclosure requires that one skilled in the art is able to determine the claimed range from the disclosure).

devices, such as electrically coupled "through [a] switching device." (Ex. 1001 49:56-64.)

Controlling a charging and discharging cycle of the first and second capacitors with first and second switching devices, respectively: In the Qualcomm litigation, no construction of this phrase was provided by the Court, instead leaving it to its plain meaning. (Ex. 1017: D.I. 243 at 40-42.) For the purposes of this petition, Petitioners agree that the broadest reasonable interpretation is the plain meaning of this phrase.

Performing a plurality of charging and discharging cycles of the first and second capacitors to generate first and second down-converted information signals across first and second impedance devices, respectively: The parties in the Qualcomm litigation do not appear to have sought construction of this phrase, leaving it to its plain meaning. (*See* Ex. 1016: D.I. 110-2.) The record from that trial, however, suggests that there was a dispute regarding the meaning of this phrase. In particular, what is meant by "to generate first and second down-converted signals across first and second impedance devices."

At trial, the defendant argued that claim 18 of the '342 patent was invalid over a portion of a textbook by DeMaw[5] (Ex. 1018). DeMaw's circuit, Figure 6.7,

[5] The DeMaw reference notes that Figure 6.7 is "similar" to a circuit suggested in Oxner, Ex. 1002. (Ex. 1018 196.) The patentee argued that one of the alleged

had a similar configuration to FIG. 16H of the '342 patent, with the switches upstream of the capacitor as shown below:

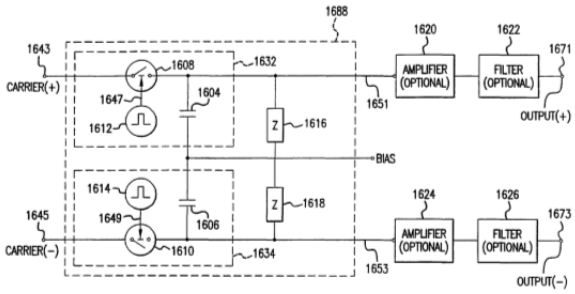

FIG.16H

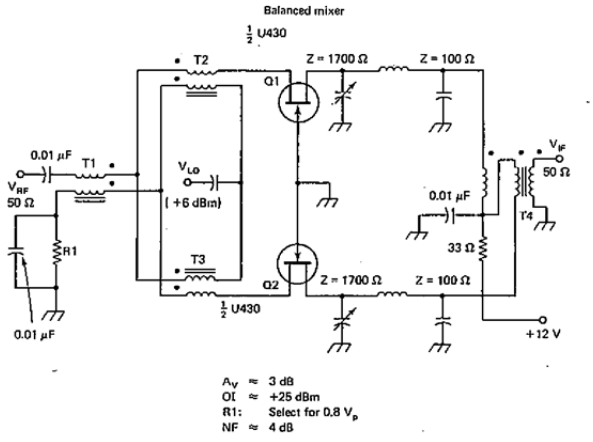

Figure 6.7 Dual FET balanced mixer using a Siliconix U430 device.

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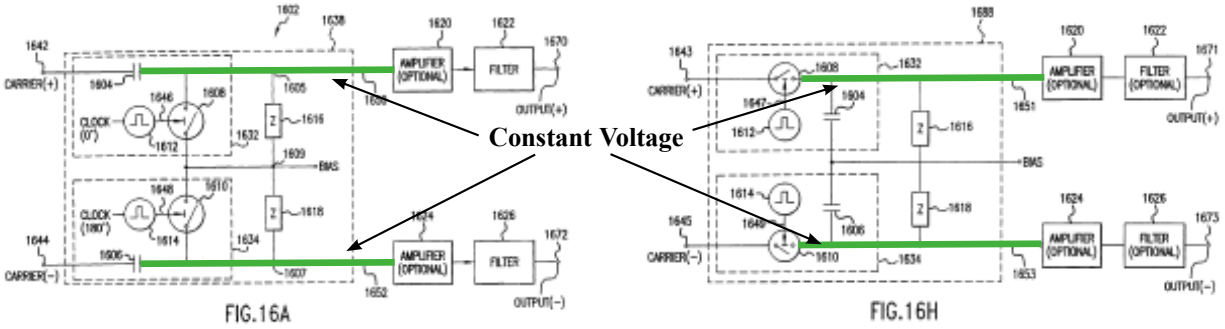
deficiencies with DeMaw was that it disclosed only an impedance value for a combination of capacitor and inductor and therefore could theoretically have been implemented with an infinite range of L and C values. (Ex. 1019: D.I. 516 at 13.) While the choice of L and C values would have no meaningful impact on how the circuit performs, Oxner includes individual values for both L and C. (Ex. 1004 6-31, Fig. 2.) Patentee also argued that defendant's expert "failed to provide clear and convincing evidence that DeMaw satisfies the 'sampling' limitation of claim 18" of the '342 patent. (Ex. 1019 at 12.) Claim 18, however, has no "sampling" limitation. (Ex. 1001 52:37-57.)

In post-trial motions, the patentee argued that DeMaw could not invalidate claim 18 of the '342 patent because defendant's expert admitted that in DeMaw the down-converted signals are first observable at the output of the switches Q1 and Q2. (Ex. 1019: D.I. 516 at 13.) This argument implies a limitation that the down-converted signal must first be generated across the impedance devices, as opposed to caused to exist across the impedance devices and first generated elsewhere. The broadest reasonable interpretation of this element in light of the specification should not be so limited.

First, the specification describes the Universal Frequency Translation (UFT) module, which is simply a switch, as performing frequency translation and thereby generating the down-converted signal in the first instance. (Ex. 1001 FIG. 1B, 6:10-11 ("The UFT modules perform frequency translation operations.")) This would have been entirely consistent with the knowledge of one of skill in the art, since it was well known that putting an input through a switch that periodically turns on and off effects frequency translation. (*See* Ex. 1020 142-43; Ex. 1002 §13.) Indeed, the patentee acknowledged in one of the provisional applications to which the '342 patent claims priority that "[h]undreds of authors have established that any harmonic function combined with a switch or other non-linear device can both up convert and down convert, preserving the information content bilaterally." (Ex. 1013 70.)

Second, while the '342 specification – in addition to stating that the UFT itself performs frequency translation -- goes on to state that "the UFT module 102 (perhaps in combination with other components) operates to generate an output signal from an input signal, where the frequency of the output signal differs from the frequency of the input signal" (Ex. 1001 6:38-41). There is nothing in the claim language or the specification that suggests that whatever other components the UFT "perhaps" works in combination with must prevent the down-converted signal from being observable upstream of the impedance devices. For example, in both FIG. 16A and 16H what are referred to in the specification as the down-converted signals (1650 and 1652 in FIG. 16A and 1651 and 1653 in FIG. 16H) are simply the voltage on a wire. (*Id.* 18:27-33, 20:5-11, 20:49-61.) It is a fundamental axiom of electrical engineering that the voltage on that wire would be effectively constant, all the way upstream to the capacitor in FIG. 16A and to the switch in FIG. 16H (Ex. 1002 §14) as shown in the annotated figures below:



Accordingly, in each of the embodiments in the specification that have the structural components necessary to meet the limitations of independent claim 18,

the respective down-converted signals are observable upstream of the impedance devices. (Ex. 1002 §14.) Patentee's implied limitation is therefore improper and the broadest reasonable interpretation in light of the specification of the phrase "to generate first and second down-converted information signals across first and second impedance devices, respectively" should be "to cause first and second down-converted information signals to exist across first and second impedance devices, respectively." *See Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1583 (Fed. Cir. 1996) ("Such an interpretation is rarely, if ever, correct and would require highly persuasive evidentiary support, which is wholly absent in this case.").

Impedance device: An impedance device according to its plain meaning is simply a device that exhibits an impedance. In the specification, a non-limiting example is given as a resistor. (Ex. 1001 18:20-24.) However, the term is not so limited and could also be a capacitor, an inductor or a combination of circuit elements.

Removing a carrier signal from the first and second down-converted information signals: The broadest reasonable interpretation of this phrase is its plain meaning. That plain meaning covers both the situation where the carrier signal is removed from the down-converted signals as a distinct step after the down-converted signals are generated as in the embodiment of FIG. 16A (Ex. 1001 18:42-50), and where the carrier signal is removed as part of the down-conversion

process as in the embodiment of FIG. 16H (*id.* 20:49-61). *Interactive Gift Exp., Inc. v. Compuserve Inc.*, 256 F.3d 1323, 1342 (Fed. Cir. 2001) ("Unless the steps of a method actually recite an order, the steps are not ordinarily construed to require one.").

VI. LEVEL OF ORDINARY SKILL IN THE ART

The level of ordinary skill in the art is evidenced by the references. *See In re GPAC Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995) (determining that the Board did not err in adopting the approach that the level of skill in the art was best determined by the references of record). The parties in the Qualcomm litigation appear to have generally agreed that one of ordinary skill in the art would have "a Bachelor's of Science degree in Electrical Engineering and four years of experience in the wireless communications industry" (Ex. 1021: D.I. 136-1 1), which is consistent with the level of skill evidenced by the cited references.

VII. STATEMENT OF MATERIAL FACTS

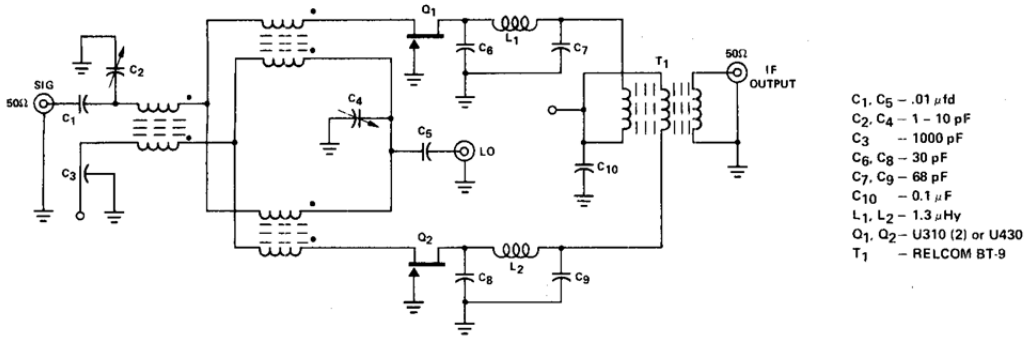
Pursuant to 37 C.F.R. § 42.22, Petitioners submit the following statement of material facts:

Oxner (Ex. 1004)

1. Oxner describes a differential circuit for down-converting an electromagnetic signal. (Ex. 1004 6-31, Fig. 2.)

2. Oxner teaches use of transformers to invert an information signal and create an inverted version of the information signal for input into a differential circuit. (*Id.*)

3. Oxner describes a first switch (Q_1) that couples the information signal to a first capacitor (C_6) and a second switch (Q_2) that couples the inverted information signal to a second capacitor (C_8). (*Id.*)



Prototype Active Balanced Mixer
Figure 2

4. Oxner describes a local oscillator (LO) which controls the opening and closing of switches Q_1 and Q_2, which in turn control charging and discharging cycles of capacitors C_6 and C_8, respectively. (*Id.* 6-31, Fig. 2, 6-33-6-34.)

5. Oxner describes use of impedance devices in the form of capacitors C_7 and C_9 across which are generated a down-converted information signal and down-converted inverted information signal. (*Id.* 6-31, Fig. 2.)

6. Oxner describes that the information signal is used to store a charge on the first capacitor (C_6) when the first switch (Q_1) is closed and that the inverted

information signal is used to store a charge on a second capacitor (C_8) when the first switch (Q_2) is closed. (*Id.* 6-35.)

7. Oxner teaches designing the IF network of his single-balanced mixer to remove the carrier signal. (*Id.* ("The IF network . . . effectively bypasses the circuit RF components (signal and local oscillator).").)

Differential Circuits (Exs. 1007, 1008, 1009)

8. The technique of mirroring a single-ended circuit around a line of symmetry in order to create a differential circuit was well known to those of ordinary skill in the art long before the filing of the '342 patent. (Ex. 1007 25-26; Ex. 1008 201-07; Ex. 1009 430-31; Ex. 1002 §6.)

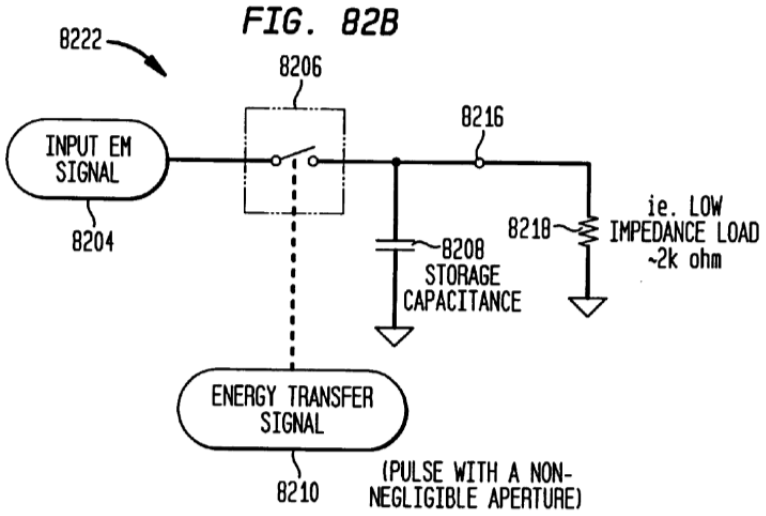
U.S. 6,061,551 (Ex. 1005)

9. The '551 patent issued on May 9, 2000, more than one year before the filing of U.S. Patent Application No. 09/855,851 ("the '851 application") on May 16, 2001. (Ex. 1001, Ex. 1005.)

10. The '851 application includes the first written description of challenged claims 18-21 and 23 of the '342 patent. (Ex. 1015.)

11. The '551 patent describes a single-ended circuit (FIG. 82B) for down-converting an electromagnetic signal with explicit values for the capacitor (18 pF)

and load resistor (2000 Ω). (Ex. 1005 FIG 82B, 67:14-25.)



12. Figure 82B of the '551 patent describes a first switch (8206) that controls charging and discharging cycles of a first capacitor (8208). (*Id.*)

13. Figure 82B of the '551 patent describes that a first information signal (8204) is used to store a charge on the first capacitor (8208). (*Id.*)

14. The '551 patent describes using the circuitry of FIG. 82B to down-convert a 900 MHz input electromagnetic signal using a sampling pulse width of 550 pico seconds. (*Id.* 67:1-13.)

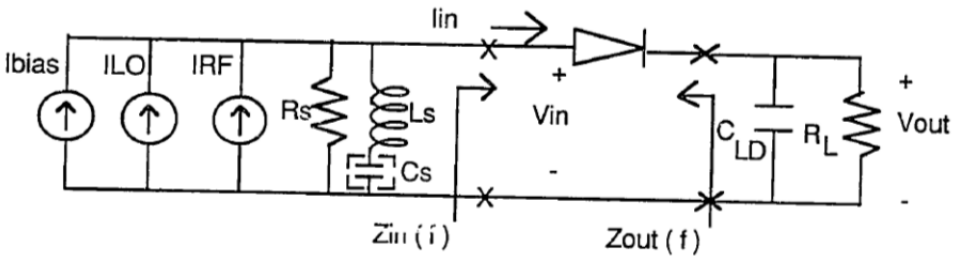
15. Example timing diagrams for this system (FIG. 82B) are presented in FIGS. 83A-F, from which one of ordinary skill in the art could have determined that sampling was occurring at n=9 with a switch off-time of approximately 9.45 ns. (*Id.* FIGS. 83A-D; Ex. 1002 §3.5)

16. It would have been known to one of ordinary skill in the art, in order to create a differential version of the single-ended circuit (FIG. 82B) of the '551 patent, to mirror the circuitry of FIG. 82B about a line of symmetry and invert the input EM signal to generate an inverted input signal using well-known techniques as described in Razavi, Thornton or Bult. (Ex. 1002 §§6-7; Ex. 1007 25-26; Ex. 1008 201-07; Ex. 1009 430-31; Ex. 1005 FIG. 82B; *cf.* Ex. 1001 FIG. 16H.)

17. Using the circuit component values and input and control signal values disclosed in the '551 patent would result in the capacitor discharging approximately 24% of its stored charge during the respective switch off times. (Ex. 1002 §3.5, eq. 3.1.)

Estabrook (Ex. 1006)

18. Estabrook describes a method of using single-ended circuit for down-converting an electromagnetic signal including a diode acting as a switch, a capacitor C_{LD} and a load resistor R_L. (Ex. 1006 37, Fig. 14.)



(a)

19. Estabrook notes that values of the capacitor and resistor may vary and provides a number of values for capacitors and resistors for different embodiments. (*Id.* 37, Fig. 14, 82, Fig. 27(b), 181, Table 16, 227, Table 26.)

20. Estabrook states that the on-time of the diode should be approximately 50% of the period of the ILO control signal in order to minimize conversion loss. (*Id.* 71, paragraph below (eq. 23).)

21. It would have been known to one of ordinary skill in the art, in order to create a differential version of the single-ended circuits (e.g. Fig. 14(a)) of Estabrook, to mirror the single-ended circuitry of Estabrook about a line of symmetry and invert the input RF signal to generate an inverted input signal using well-known techniques as described in Razavi, Thornton or Bult. (Ex. 1002 § ; Ex. 1006 37, Fig. 14; Ex. 1007 25-26; Ex. 1008 201-07; Ex. 1009 430-31; *cf.* Ex. 1001 FIG. 16H.)

22. Using the circuit component values and input and control signal values disclosed in Estabrook for Figure 14 (T_{off} = 0.55 ns, R = 1000 Ω, C = 2.8 pF) would result in each capacitor discharging approximately 18% of its stored charge during the respective diode off times. (Ex. 1006 37, Fig. 14; Ex. 1002 §3.6, eq. 3.1.)

23. Using the circuit component values and input and control signal values disclosed in Estabrook for Figure 27(b) (T_{off} = 0.55 ns, R = 500 Ω, C = 2.8

pF) would result in the capacitor discharging approximately 33% of its stored charge during the respective diode off times. (Ex. 1006 82, Fig. 27(b); Ex. 1002 eq. 3.1.)

24. Using the circuit component values and input and control signal values disclosed in Estabrook Table 16 would result in each capacitor discharging approximately 18% (T_{off} = 0.55 ns, R = 1000 Ω, C = 2.8 pF) or 12% (T_{off} = 0.55 ns, R = 1500 Ω, C = 2.8 pF) of its stored charge during the respective diode off times, depending on the type of diode used. (Ex. 1006 181, Table 16; Ex. 1002 eq. 3.1.)

25. Using the circuit component values and input and control signal values disclosed in Estabrook Table 26 for direct down-conversion would result in each capacitor discharging approximately 31% (T_{off} = 0.55 ns, R = 500 Ω, C = 3.1 pF) or 12.5% (T_{off} = 0.55 ns, R = 1500 Ω, C = 3.1 pF) of its stored charge during the respective diode off times, depending on the type of diode used. (Ex. 1006 227, Table 26; Ex. 1002 eq. 3.1.)

VIII. IDENTIFICATION OF HOW THE CHALLENGED CLAIMS ARE UNPATENTABLE

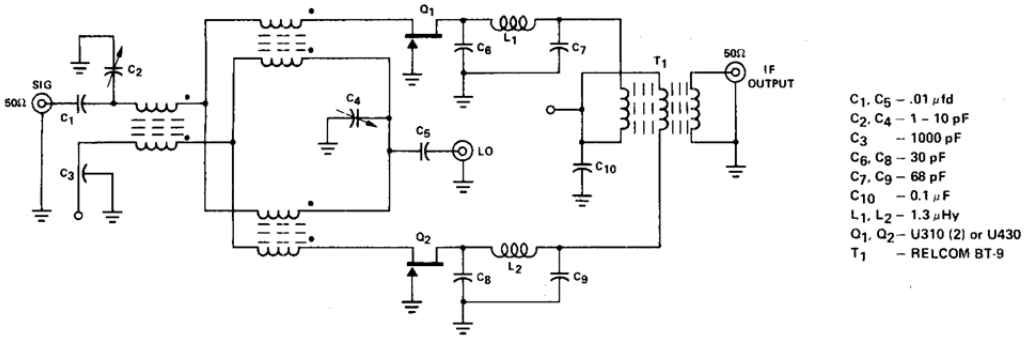
Pursuant to Rule 42.104(b)(4)-(5), this section demonstrates that the challenged claims are unpatentable.

A. Claims 18 and 23 are Anticipated by Oxner under 35 U.S.C. § 102 (b)

The following subsections explain on an element-by-element basis how Oxner discloses the subject matter encompassed by claims 18 and 23 of the '342 patent.

Claim 18: "A method for down-converting an electromagnetic signal, comprising the steps of:

Oxner discloses a method for down-converting an electromagnetic signal using the apparatus shown in Figure 2. (Ex. 1004 6-31, Figure 2.)



Prototype Active Balanced Mixer
Figure 2

Claim 18: "(1) receiving an information signal;"

Oxner describes receiving an information signal, labeled "SIG" in Figure 2. (*Id.*)

Claim 18: "(2) inverting the information signal to generate an inverted information signal;"

Oxner describes transformers that "Maintain a differential phase of 180º across the symmetrical balanced loads" (i.e., inverting the information signal to generate an inverted information signal.) (*Id.* 6-31, Fig. 2, 6-34 "Designing the Input Transformer".)

Claim 18: "(3) electrically coupling the information signal to a first capacitor and the inverted information signal to a second capacitor;"

Oxner describes electrically coupling the information signal to a first capacitor (C_6) through switch Q_1 and electrically coupling the inverted information signal to a second capacitor (C_8) through switch Q_2. (*Id.* 6-31, Fig. 2.)

Claim 18: "(4) controlling a charging and discharging cycle of the first and second capacitors with first and second switching devices electrically coupled to the first and second capacitors, respectively; and"

In Figure 2 of Oxner, "the JFET mixer acts as a switch, with the local oscillator acting as the switch drive signal." (*Id.* 6-30.) Switch Q_1 is electrically coupled to capacitor C_6 and switch Q_2 is electrically coupled to capacitor C_8. (*Id.* 6-31, Fig. 2.) Switch Q_1 controls the charging and discharging cycles of capacitor C_6 and switch Q_2 controls the charging and discharging cycles capacitor C_8. (*Id.;* Ex. 1002 § 3.1) This behavior is confirmed by simulation of the circuit of Figure 2. (Ex. 1002 Fig. 3.1.)

Claim 18: "(5) performing a plurality of charging and discharging cycles of the first and second capacitors to generate first and second down-converted information signals across first and second impedance devices, respectively;"

The LO control signal in Oxner Figure 2 causes switches Q_1 and Q_2 to open and close each LO cycle and results in repeated charging and discharging cycles across capacitors C_6 and C_8. (Ex. 1004 6-31, Fig. 2; Ex. 1002 §3.1.) As a result of these repeated charging and discharging cycles a down-converted information signal is generated across a first impedance device (capacitor C_7) and a down-converted inverted information signal is generated across a second impedance device (capacitor C_9). (Ex. 1004 6-31, Fig. 2; Ex. 1002 §3.1)

Claim 18: "wherein the information signal is used to store a charge on the first capacitor when the first switching device is closed and the inverted information signal is used to store a charge on the second capacitor when the second switching device is closed."

In Oxner Figure 2, when the first switch (Q_1) is closed the information signal is used to store a charge the first capacitor (C_6) and when the second switch (Q_2) is closed the inverted information signal is used to store a charge the second capacitor (C_8). (Ex. 1004 6-31, Fig. 2; Ex. 1002 §3.1.)

Claim 23: "The method of claim 18, further comprising the step of: removing a carrier signal from the first and second down-converted information signals."

Oxner teaches designing the IF network of his single-balanced mixer to remove the carrier signal. (Ex. 1004 6-35 ("The IF network . . . effectively bypasses the circuit RF components (signal and local oscillator)."); *see also* Ex. 1002 §3.13.)

* * *

Thus, claims 18 and 23 are anticipated under 35 U.S.C. § 102(b) by Oxner.

B. Claims 18, 19, 20, 21, and 23 are rendered obvious under 35 U.S.C. § 103 by the '551 patent in view of knowledge of one of ordinary skill in the art, as evidenced by Razavi, Thornton or Bult.

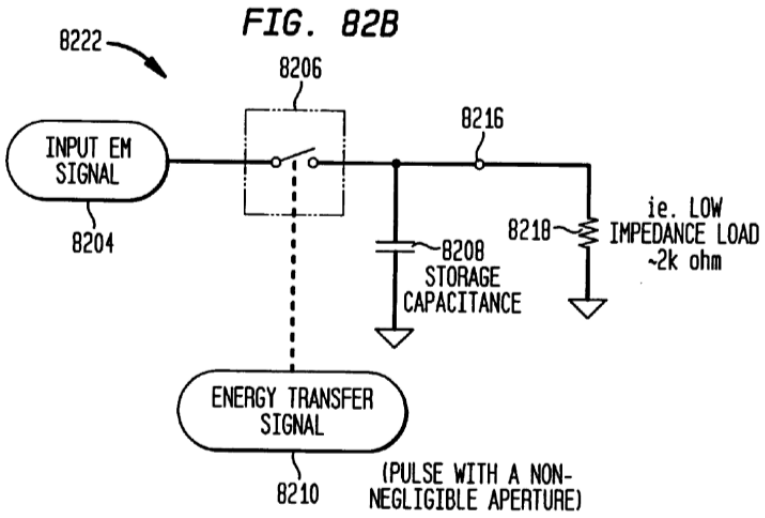
The following subsections explain on an element-by-element basis how claims 18-21, and 23 of the '342 patent are rendered obvious by the '551 patent in view of knowledge of one of ordinary skill in the art, as evidenced by Razavi, Thornton or Bult.

Claim 18: "A method for down-converting an electromagnetic signal, comprising the steps of:

The '551 patent discloses a method for down-converting an electromagnetic signal. (Ex. 1005 Abstract.)

Claim 18: "(1) receiving an information signal;"

The '551 patent discloses receiving an information signal, for example, the input EM signal 8204 in FIG. 82B. (Ex. 1005 FIG. 82B.)



Claim 18: "(2) inverting the information signal to generate an inverted information signal;"

It would have been obvious to one of skill in the art to mirror the circuit of FIG. 82B of the '551 patent around a line of symmetry and invert the input EM signal to generate an inverted input and to create a differential version of the circuit as well known in the art and reflected in Razavi, Thornton, or Bult. (Ex. 1007 25-26; Ex. 1008 201-07; Ex. 1009 430-31; Ex. 1002 §§6-7.)

Claim 18: "(3) electrically coupling the information signal to a first capacitor and the inverted information signal to a second capacitor;"

The '551 patent describes electrically coupling the information signal to a first capacitor, storage capacitance 8208 through switch 8206. (Ex. 1005 FIG. 82B.) The mirrored version of FIG. 82B in a differential circuit would be identical and would couple the inverted information signal to a second capacitor through a second switch. (Ex. 1002 §§6-7.)

Claim 18: "(4) controlling a charging and discharging cycle of the first and second capacitors with first and second switching devices electrically coupled to the first and second capacitors, respectively; and"

The '551 patent describes controlling a charging and discharging cycle of the storage capacitor 8208 using switch 8206. (Ex. 1005 FIGS. 82B, 83C-E, 85:40-58, FIG. 57E.) The mirrored version of FIG. 82B in a differential circuit would be identical and would control a charging and discharging cycle of a second capacitor using a second switch. (Ex. 1002 §§6-7.)

Claim 18: "(5) performing a plurality of charging and discharging cycles of the first and second capacitors to generate first and second down-converted information signals across first and second impedance devices, respectively;"

The '551 patent describes performing a plurality of charging and discharging of a first capacitor 8208 to generate a first down-converted information signal across a first impedance device, the low impedance load 8218, which is a 2000 Ω resistor. (Ex. 1005 FIGS. 82B, 83C-E, 85:40-58.) The mirrored version of FIG. 82B in a differential circuit would be identical and would perform a plurality of charging and discharging of a second capacitor to generate a second down-converted information signal across a second impedance device. (Ex. 1002 §§6-7.)

Claim 18: "wherein the information signal is used to store a charge on the first capacitor when the first switching device is closed and the inverted information signal is used to store a charge on the second capacitor when the second switching device is closed."

The '551 patent describes that the information signal, input EM signal 8204, is used to store a charge on a first capacitor, storage capacitance 8208, when a first switching device 8206 is closed. (Ex. 1005 FIGS. 82B, 83C-E, 85:40-58.) The mirrored version of FIG. 82B in a differential circuit would be identical and the inverted information signal would be used to store a charge on a second capacitor when a second switching device is closed. (Ex. 1002 §§6-7.)

Claim 19: "The method of claim 18, wherein the first capacitor discharges between six percent to fifty percent of the total charge stored therein during a period of time that the first switching device is open, and wherein the second capacitor discharges between six percent to fifty percent of the total charge stored therein during a period of time that the second switching device is open."

Using the circuit component values and input and control signal values disclosed in the '551 patent would result in each capacitor discharging approximately 24% of its stored charge during the respective switch off times. (Ex. 1002 §3.5.)

Claim 20: "The method of claim 18, wherein the first capacitor discharges between ten percent to twenty-five percent of the total charge stored therein during a period of time that the first switching device is open, and wherein the second capacitor discharges between ten percent to twenty-five percent of the total charge stored therein during a period of time that the second switching device is open."

Using the circuit component values and input and control signal values disclosed in the '551 patent would result in each capacitor discharging

approximately 24% of its stored charge during the respective switch off times. (Ex. 1002 §3.7.)

Claim 21: "The method of claim 18, wherein the first capacitor discharges between fifteen percent to thirty percent of the total charge stored therein during a period of time that the first switching device is open, and wherein the second capacitor discharges between fifteen percent to thirty percent of the total charge stored therein during a period of time that the second switching device is open."

Using the circuit component values and input and control signal values disclosed in the '551 patent would result in each capacitor discharging approximately 24% of its stored charge during the respective switch off times. (Ex. 1002 §3.9.)

Claim 23: "The method of claim 18, further comprising the step of: removing a carrier signal from the first and second down-converted information signals."

The '551 patent describes removing the carrier signal from the down-converted signal as part of the down-conversion process. (Ex. 1004 FIGS. 83A-F, 67:48-68:4.) The mirrored version of FIG. 82B in a differential circuit would be identical and would also remove the carrier signal as part of the down-conversion process. (Ex. 1002 §3.12.)

* * *

Thus, claims 18, 19, 20, 21, and 23 are rendered obvious under 35 U.S.C. § 103 by the '551 patent in view of knowledge of one of ordinary skill in the art, as evidenced by Razavi, Thornton or Bult.

C. Claims 18, 19, 20, 21, and 23 are rendered obvious under 35 U.S.C. § 103 by Estabrook in view of knowledge of one of ordinary skill in the art, as evidenced by Razavi, Thornton or Bult.

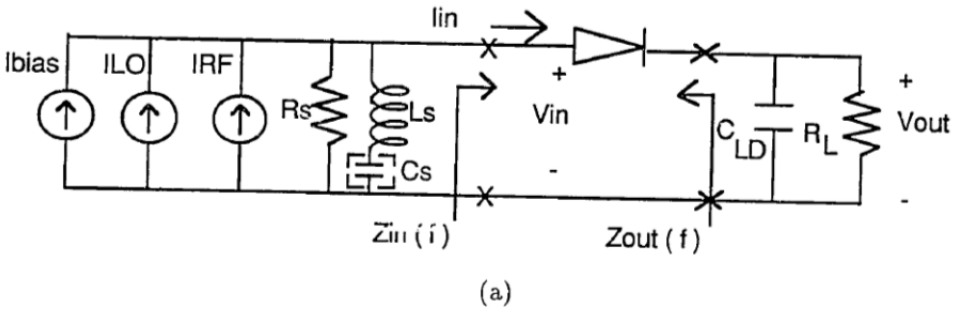
The following subsections explain on an element-by-element basis how claims 18, 19, 20, 21, and 23 of the '342 patent are rendered obvious by Estabrook in view of knowledge of one of ordinary skill in the art, as evidenced by Razavi, Thornton or Bult.

Claim 18: "A method for down-converting an electromagnetic signal, comprising the steps of:"

Estabrook discloses a method for down-converting an electromagnetic signal. (Ex. 1006 37, Fig. 14.) "The circuit shown in Figure 14(a) was chosen as a beginning point for the design of the mixer in the direct downconversion receiver…." (*Id.* 44, last paragraph.)

Claim 18: "(1) receiving an information signal;"

Estabrook discloses receiving an information signal, IRF in Figure 14. (*Id.* 37.)



(a)

Claim 18: "(2) inverting the information signal to generate an inverted information signal;"

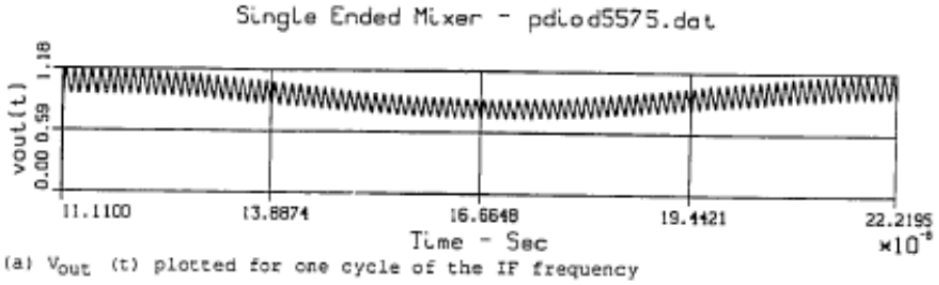
It would have been obvious to one of skill in the art to mirror the single-ended circuits of Estabrook around a line of symmetry and invert the input IRF to generate an inverted input and create a differential version of the circuit as well known in the art and reflected in Razavi, Thornton or Bult. (Ex. 1007 25-26; Ex. 1008 201-07; Ex. 1009 430-31; Ex. 1002 §§6, 8.)

Claim 18: "(3) electrically coupling the information signal to a first capacitor and the inverted information signal to a second capacitor;"

Estabrook describes electrically coupling the information signal to a first capacitor through a diode. (Ex. 1006 37, Fig. 14(a).) The mirrored version of Figure 14(a) in a differential circuit would be identical and would couple the inverted information signal to a second capacitor through a second diode. (Ex. 1002 §§6, 8.)

Claim 18: "(4) controlling a charging and discharging cycle of the first and second capacitors with first and second switching devices electrically coupled to the first and second capacitors, respectively; and"

Estabrook describes controlling a charging and discharging cycle of the first capacitor with a first switching device in the form of a diode. (Ex. 1006 37, Fig. 14.) The charging and discharging of the capacitor is shown in Figure 16(a). (*Id.* 48, Fig 16(a).)



(a) V_{out} (t) plotted for one cycle of the IF frequency

The mirrored version of Figure 14(a) in a differential circuit would be identical and would control a charging and discharging cycle of a second capacitor using a second diode. (Ex. 1002 §§6, 8.)

Claim 18: "(5) performing a plurality of charging and discharging cycles of the first and second capacitors to generate first and second down-converted information signals across first and second impedance devices, respectively;"

Estabrook describes performing a plurality of charging and discharging cycles of the first capacitor resulting in the generation of a first down-converted signal across a first impedance device, the load resistor R_L. (Ex. 1006 37, Fig. 14; *see also id.* 34, first full paragraph ("The output signal is taken as the voltage on the load resistor R_L.").) The mirrored version of Figure 14 in a differential circuit would be identical and would perform a plurality of charging and discharging

cycles of a second capacitor resulting in generation of a second down-converted signal across a second impedance device. (Ex. 1002 §§6, 8.)

Claim 18: "wherein the information signal is used to store a charge on the first capacitor when the first switching device is closed and the inverted information signal is used to store a charge on the second capacitor when the second switching device is closed."

Estabrook describes that the information signal, IRF, is used to store a charge on a first capacitor, C_{LD}, when a first switching device (the diode) is on or closed. (Ex. 1006 37, FIG. 14.) The mirrored version of Figure 14 in a differential circuit would be identical and the inverted information signal would be used to store a charge on a second capacitor when a second switching device is closed. (Ex. 1002 §§6, 8.)

Claim 19: "The method of claim 18, wherein the first capacitor discharges between six percent to fifty percent of the total charge stored therein during a period of time that the first switching device is open, and wherein the second capacitor discharges between six percent to fifty percent of the total charge stored therein during a period of time that the second switching device is open."

Using the circuit component values and input and control signal values disclosed in Figure 14 of Estabrook would result in each capacitor discharging approximately 18% of its stored charge during the respective diode off times. (Ex. 1006 37, Fig. 14; Ex. 1002 §3.6.) Using the circuit component values and input and control signal values disclosed in Figure 27(b) of Estabrook (T_{off} = 0.55 ns, R = 500 Ω, C = 2.8 pF) would result in each capacitor discharging approximately

33% of its stored charge during the respective diode off times. (Ex. 1006 82, Fig. 27(b); Ex. 1002 eq. 3.1.) Using the circuit component values and input and control signal values disclosed in Estabrook Table 16 would result in each capacitor discharging approximately 18% (T_{off} = 0.55 ns, R = 1000 Ω, C = 2.8 pF) or 12% (T_{off} = 0.55 ns, R = 1500 Ω, C = 2.8 pF) of its stored charge during the respective diode off times, depending on the type of diode used. (Ex. 1006 181, Table 16; Ex. 1002 eq. 3.1.) Using the circuit component values and input and control signal values disclosed in Estabrook Table 26 for direct down-conversion would result in each capacitor discharging approximately 31% (T_{off} = 0.55 ns, R = 500 Ω, C = 3.1 pF) or 12.5% (T_{off} = 0.55 ns, R = 1500 Ω, C = 3.1 pF) of its stored charge during the respective diode off times, depending on the type of diode used. (Ex. 1006 227, Table 26; Ex. 1002 eq. 3.1.)

Claim 20: "The method of claim 18, wherein the first capacitor discharges between ten percent to twenty-five percent of the total charge stored therein during a period of time that the first switching device is open, and wherein the second capacitor discharges between ten percent to twenty-five percent of the total charge stored therein during a period of time that the second switching device is open."

Using the circuit component values and input and control signal values disclosed in Figure 14 of Estabrook would result in each capacitor discharging approximately 18% of its stored charge during the respective diode off times. (Ex. 1006 37, Fig. 14; Ex. 1002 §3.8.) Using the circuit component values and input and control signal values disclosed in Estabrook Table 16 would result in each

capacitor discharging approximately 18% (T_{off} = 0.55 ns, R = 1000 Ω, C = 2.8 pF) or 12% (T_{off} = 0.55 ns, R = 1500 Ω, C = 2.8 pF) of its stored charge during the respective diode off times, depending on the type of diode used. (Ex. 1006 181, Table 16; Ex. 1002 eq. 3.1.) Using the circuit component values and input and control signal values disclosed in Estabrook Table 26 for direct down-conversion with a C_{jo} of 0.25 pF would result in each capacitor discharging approximately12.5% (T_{off} = 0.55 ns, R = 1500 Ω, C = 3.1 pF) of its stored charge during the respective diode off times. (Ex. 1006 227, Table 26; Ex. 1002 eq. 3.1.)

Claim 21: "The method of claim 18, wherein the first capacitor discharges between fifteen percent to thirty percent of the total charge stored therein during a period of time that the first switching device is open, and wherein the second capacitor discharges between fifteen percent to thirty percent of the total charge stored therein during a period of time that the second switching device is open."

Using the circuit component values and input and control signal values disclosed in Figure 14 of Estabrook would result in each capacitor discharging approximately 18% of its stored charge during the respective diode off times. (Ex. 1006 37, Fig. 14; Ex. 1002 §3.10.) Using the circuit component values and input and control signal values disclosed in Estabrook Table 16 for *idoide1010* and *idiod2362* would result in each capacitor discharging approximately 18% (T_{off} = 0.55 ns, R = 1000 Ω, C = 2.8 pF) of its stored charge during the respective diode off times. (Ex. 1006 181, Table 16; Ex. 1002 eq. 3.1.)

Claim 23: "The method of claim 18, further comprising the step of:

removing a carrier signal from the first and second down-converted information signals."

The down-conversion circuits described in Estabrook have a low-pass filtering effect that simultaneously removes the carrier signal while down-converting the first and second information signals. (Ex. 1002 §3.14.) This is confirmed by FFT plots of the output showing that the amplitude of the RF signal has been greatly reduced in the output. (Ex. 1006 56, Fig. 19.)

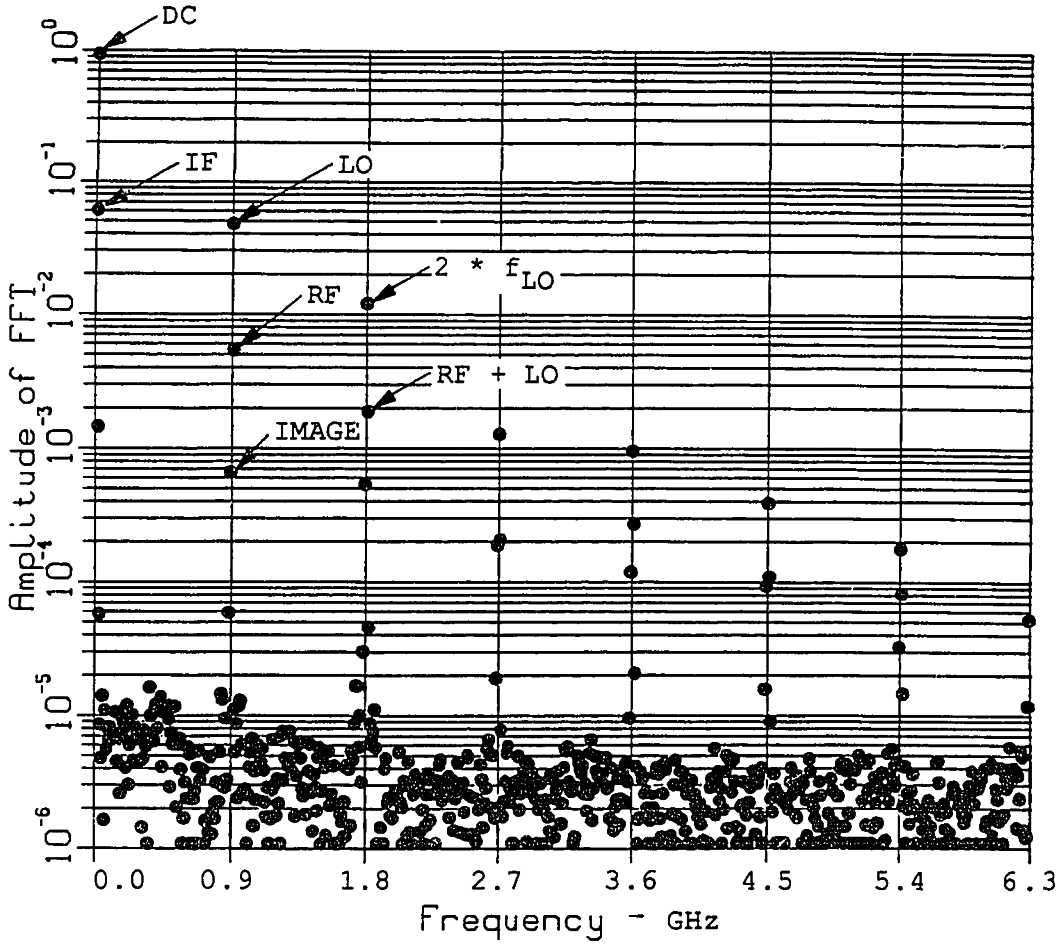


Figure 19: Spectrum of V_{out} - *Resistively Matched* mixer.

* * *

Thus, claims 18, 19, 20, 21, and 23 are rendered obvious under 35 U.S.C. § 103 by Estabrook in view of knowledge of one of ordinary skill in the art, as evidenced by Razavi, Thornton or Bult.

IX. CONCLUSION

For the foregoing reasons, Petitioners ask that *inter partes* review of the '342 patent be instituted and that claims 18, 19, 20, 21, and 23 be rejected.

Respectfully submitted,

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EXHIBIT APPENDIX

Exhibit	Description
1001	U.S. Patent No. 7,496,342 (for *inter partes* review)
1002	Declaration of Dr. Asad Abidi
1003	CV of Dr. Abidi
1004	Ed Oxner, "Application Note: FETs in Balanced Mixers," Siliconix Inc. 1979.
1005	U.S. Patent No. 6,061,551
1006	"The direct conversion receiver: Analysis and design of the front-end components," (Ph.D diss., Stanford University, 1989).
1007	Behzad Razavi, "Principles of Data Conversion System Design," IEEE Press 1995, Chapter 2: Basic Sampling Circuits.
1008	Richard D. Thornton et al., "Multistage Transistor Circuits: Semiconductor Electronics Education Committee, Volume 5," John Wiley & Sons Inc. 1965, pp. 201-07.
1009	Klaas Bult and Hans Wallinga, "A CMOS Four-Quandrant Analog Multiplier," *IEEE Journal of Solid-State Circuits*, Vol. SC-21, No. 3, June 1986, 430-35.
1010	D.I. 152-1: Plaintiff ParkerVision Inc.'s Supplemental Disclosure of Asserted Claims and Infringement Contentions Based Upon Qualcomm's Belated Supplementation of Its Interrogatory Responses to Identify Additional Accused Instrumentalities.
1011	U.S. Patent No. 7,515,896
1012	U.S. Provisional Application No. 60/204,796.
1013	U.S. Provisional Application No. 60/213,363.
1014	U.S. Provisional Application No. 60/272,043.
1015	U.S. Patent Application No. 09/855,851.
1016	D.I. 110: Joint Claim Construction Statement.
1017	D.I. 243: February 20, 2013 Order of Judge Roy B. Dalton, United States District Court, Middle District of Florida, Jacksonville Division.
1018	Doug DeMaw, "Practical RF Design Manual," Prentice-Hall Inc. 1982, Chapter 6: Mixers, Balanced Modulators and Detectors.
1019	D.I. 516: ParkerVision's Response in Opposition to Qualcomm's Renewed Motion for Judgment as a Matter of Law and Motion for New Trial Regarding Invalidity.
1020	Henry J. Zimmermann and Samuel J. Mason, "Electronic Circuit

	Theory: Devices, Models, and Circuits," John Wiley & Sons, Inc., 1959, pp. 142-44.
1021	D.I. 136-1: Declaration of Paul Prucnal, Ph.D. in Support of Plaintiff ParkerVision, Inc.'s Rebuttal Claim Construction Brief.
1022	United States Patent Application No. 09/550,644: Originally filed claims.
1023	"U440/441 Matched N-Channel JFET Pairs," Siliconix, Data Sheet P-37405-Rev.D, 1994.
1024	S.A. Schelkunoff and H.T. Friis, "Antennas: Theory and Practice," New York: Wiley, 1952.
1025	United States Patent No. 3,241,078.
1026	K.K. Clarke and D.T. Hess, "Communications Circuits: Analysis and Design," Addison-Wesley 1971.

CERTIFICATE OF SERVICE

I hereby certify that, on July 2, 2014, I caused a true and correct copy of the foregoing Petition for *Inter Partes Review* of U.S. Patent No. 7,496,342, in its entirety, to be served via UPS, next day delivery on the following:

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