# PRACTICAL RF DESIGN MANUAL

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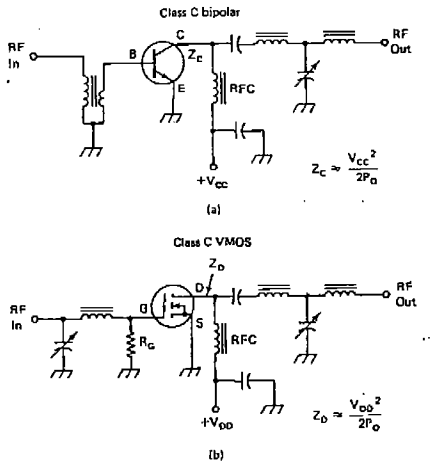



**Figure 4.3** Class C amplifiers that use (a) a bipolar transistor and (b) a VMOS FET.

Figure 4.3 shows how a bipolar transistor and a VMOS power FET compare in terms of circuit arrangement for class C operation. Forward bias is not used in either example. $R_G$ is selected for the circuit of Fig. 4.3(b) according to the driving power available. That is, there must be sufficient available drive to develop the required $V_{GS}$ swing across $R_G$ for full output power from the amplifier. In the interest of stability it is wise to use the lowest value of resistance possible at $R_G$. Values from 50 to 1000 Ω are typical.

The value of drain impedance is determined in the same manner as for a bipolar transistor collector impedance. A close approximation can be obtained from

$$Z_o = \frac{V_{CC}^2}{2P_o} \ \Omega \quad \text{or} \quad Z_o = \frac{V_{DD}^2}{2P_o} \ \Omega$$

where $P_o$ is the anticipated output power in watts. A more precise determination requires knowledge of the actual collector-to-emitter voltage ($V_{CE}$) with drive applied to the amplifier. Similarly, we need to know the actual $V_{DS}$ for a power FET in the interest of reasonable accuracy. This will be dependent on the $R_{DS(on)}$ characteristic of the



power FET, which is the resistance of the drain-source junction when the transistor is fully conducting. For a VMOS power FET this is on the order of 0.5 Ω, and we can use that number for most of our calculations. Now our equation for $Z_o$ becomes

$$Z_o = \frac{[V_{DD} - V_{DS(on)}]^2}{2P_o} \ \Omega$$

To find the value of $V_{DS(on)}$, we will consider it equal to

$$V_{DS(on)} = R_{DS(on)} \times I_D \text{ volts}$$

The results of these equations can be demonstrated by choosing some values for a hypothetical VMOS amplifier. Assume we apply a 24-V $V_{DD}$ to a selected transistor, Q1. It will have an $I_D$ of 3 A and a power output of 72 W. Thus for a $R_{DS}$ of 0.5 Ω,

$$V_{DS(on)} = 0.5 \times 3 = 1.5 \text{ V}$$

Therefore, the $Z_o$ of the amplifier will be

$$Z_o = \frac{(24 - 1.5)^2}{144} = 3.5 \ \Omega$$

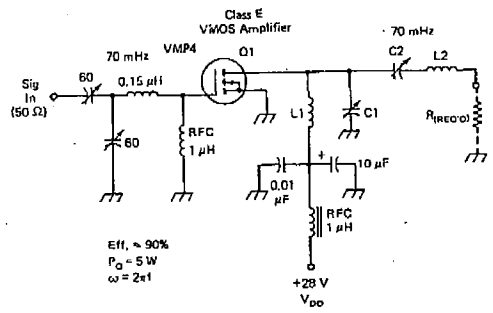
This will be the load line we use when designing our matching networks. VMOS amplifier efficiencies of 65% or greater are typical for the linear class A or B modes.

#### 4.1.2 VMOS Class E Amplifier

Efficiencies as great as 90% can be obtained by operating bipolar or VMOS power transistors in the class E mode. The virtues of operating the devices in this switching mode are low power dissipation, high efficiency, insensitivity to component tolerances, and low junction temperature. Figure 4.4 shows a class E circuit that uses a Siliconix VMP4 power FET. The network $Q_L$ for amplifier testing was 3. The equations in Fig. 4.4 are based on the papers by N. Sokal, referenced in the bibliography section of this chapter.

## 4.2 MATCHING NETWORKS

We acknowledged earlier in this chapter that maximum power transfer will occur only if the amplifier device is matched correctly to its source and load impedances. Therefore, it becomes an important design consideration to select networks that are suitable for this and the stability requirements of the amplifier. Fundamentally, the design approach re-




1. $Q_L \geq 1.7879$

2. $R_{(REQ'D)} = 0.5768 \left(\frac{V_{DD} - V_{DS}}{P}\right)$

3. $L2 = \frac{Q_L R}{\omega}$

4. $C2 = \frac{1}{\omega Q_L R}\left[1 + \frac{1.110}{Q_L - 1.7879}\right]$

5. $L1 \geq \frac{10}{\omega^2 C1}$

6. $C1 = \frac{0.1636}{\omega R}\left[1 + \frac{0.81\,Q_L}{Q_L^2 + 4} + \frac{0.7}{\omega^2 L1}\right]$

**Figure 4.4** Details of a class E VMOS amplifier with network equations developed by N. Sokal of Design Automation Corp.

mains the same, irrespective of the class of operating mode. The notable exception is in the case of the class E amplifier described in Fig. 4.4.

Matching networks can be narrow band or broadband, depending on our requirements. The former usually consist of variable-$C$ components and a fixed inductance, but in some instances the designer may elect to make both the $L$ and $C$ network components variable. This allows great latitude in effecting a matched condition when such unknown factors as input and output capacitance must be addressed. A totally adjustable network of this type is sometimes called a "sloppy network." Adjustment proceeds along purely empirical lines once the network values are arrived at by means of approximation. Unfortunately, the foregoing technique is the rule rather than the exception when working with power bipolar transistors, except for class E amplifiers, where a substantial amount of leeway is acceptable. Empirical adjustment is necessary because of the variations in transistor characteristics for various brands of the same transistor type number. Also, many data sheets do not provide meaningful information concerning the input and output capacitances, especially at various operating frequencies. This is not a problem with VMOS power FETs, and relates primarily to bipolar devices. The totally adjustable network allows the designer to compensate also for stray inductive and capacitive reactances that are always present in a solid-state amplifier circuit.



Most broadband amplifiers contain $LC$ filters of the low-pass or bandpass variety. The wide-band filters are usually accompanied by broadband matching transformers of the toroidal kind. Other broadband amplifiers contain no selective filter elements and utilize nothing more than broadband transformers.

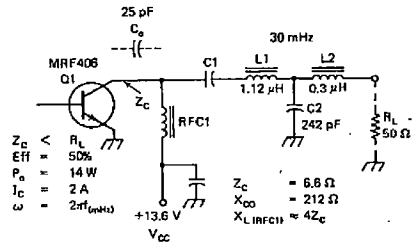
### 4.2.1 Narrow-Band Networks

There is an essential difference in the design approach between vacuum-tube and solid-state amplifiers when using narrow-band networks. In the interest of waveform purity in a tube type of amplifier, the general practice is to design the network for high loaded $Q$, typically between 10 and 15. A somewhat different situation prevails when working with semiconductors: owing to the very high gain of most modern transistors, lower network $Q$s become almost mandatory to ensure amplifier stability. Engineers have found that a maximum network $Q$ of 5 is the most viable. The waveform is usually purified to an acceptable level by adding harmonic filters at the amplifier output. Often it is sufficient to use an inexpensive half-wave type of filter for this purpose.

The pi-network turns out to be impractical for use in most high-power solid-state amplifiers. Although network values can be reached by application of the standard equations, the resultant component values usually become impractical, especially as the operating frequency is increased to the high-frequency part of the spectrum and above. The inductance values often become a small fraction of a microhenry, and the capacitance values increase to proportions that make the use of variable capacitors beyond reason.

A more suitable approach is seen in the T-network of Fig. 4.5. This circuit provides the desired low-pass response and yields practical values of $L$ and $C$, even at 30 MHz. The T-network is especially suited to low values of $Z_C$ that must be transformed to higher values of impedance, such as 50 Ω.

The network equations are included in Fig. 4.5, along with the answers based on the circuit values noted in the drawing. In the example we have assumed an amplifier efficiency of 50% and a $Q_L$ of 4. The operating frequency is 30 MHz, and $I_C$ at peak power output is 2 A. $C_o$ is the transistor output capacitance at 30 MHz. This characteristic is usually available from the manufacturer. $C1$ should have an $X_c$



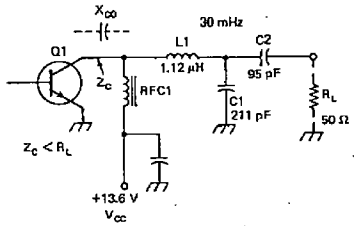

1. Select a $Q_L$ (4)
2. $X_{L1} = Z_C Q_L + X_{CO} = 238.4\ \Omega$
   $X_{L2} = R_L \times B = 55.75\ \Omega$
   Where $B = \sqrt{\frac{A}{R_L}} - 1 = 1.115$
3. and $A = Z_C\ (Q_L^2 + 1) = 112.2$
4. $X_{C2} = \frac{A}{Q_L + B} = 21.93\ \Omega$
5. $L_{\mu H} = \frac{X_L}{\omega}$
6. $C_{pF} = \frac{1}{\omega X_C}$

**Figure 4.5** T-network design procedure for a collector matching circuit.

of 10 or less. Ceramic-chip capacitors are preferred at $C1$ in the interest of minimum series inductance and related phase shifts. $C2$ can be made variable to ensure precise adjustment of the network $C$ in the presence of stray capacitance. This network is suitable for use at the input of $Q1$. $L1$ and $L2$ can be variable elements along with $C2$, hence permitting precise matching with the aid of an input VSWR meter.

A network that is particularly popular in VHF amplifiers, but works well at lower frequencies as well, is presented in Fig. 4.6. Like the circuit of Fig. 4.5, it is used when the $Z_C$ is lower in magnitude than $R_L$. We can see that it closely resembles the conventional $L$ network, except that $C2$ has been added to permit greater matching range and ease. A low-pass response is obtained from this network, an aid to the suppression of harmonic currents. Assume that the operating parameters for this amplifier are identical with those in Fig. 4.5. The reactances obtained from the equations of Fig. 4.6 are based on that premise. At the higher frequencies it is common practice to make both $C1$ and $C2$ variable. The values noted in the circuit for $C1$, $C2$, and $L1$ are the calculated values, but do not include stray $C$ and $L$ components.






1. $X_{L1} = (Z_C Q_L) + X_{CO} = 238.4\ \Omega$
2. $X_{C2} = AR_L = 55.75\ \Omega$, where
   $A = \sqrt{\left[\frac{Z_C\ (Q_L^2 + 1)}{R_L}\right]} - 1 = 1.115$
3. $X_{C1} = \frac{B}{Q_L A} = 25.15\ \Omega$, where
   $B = Z_C\ (Q_L^2 + 1) = 112.2$

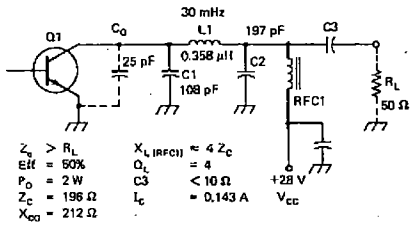
**Figure 4.6** Design format for a modified L network used to match the amplifier to its load.

In situations where $Z_C$ is greater in value than $R_L$, a pi network can be used effectively for matching purposes. This is shown in Fig. 4.7, where $Z_C$ is 196 Ω and $R_L$ is 50 Ω. Note that the operating conditions for this circuit are different from those of Figs. 4.5 and 4.6. $V_{CC}$ has become +28 V, $I_C$ is 0.143 A, and $P_o$ is 2 W. This results in a collector impedance of approximately 196 Ω. In a practical circuit, $C1$ and $C2$ can be made variable.

The three networks described in this section can be used for interstage coupling and need not be used as shown. If the impedance levels are such that the equations provide impractical component values, a broadband transformer can be used between the transistor and the network to change the transformation ratio to a more workable value.

A tapped-coil narrow-band matching network can be an alternative to the three methods just described. This approach is seen in Fig. 4.8, where $L1$ is tapped for a low impedance to match the characteristic $Z$ of the signal source. $C1$ and $L1$ form a resonator and provide the desired selectivity. $L2$ is wound over the ground or cold end of $L1$, using the proper number of turns to ensure a matched condition between the signal source and the base of $Q1$. The $LC$ ratio provided by $C1$ and $L1$ is not critical as long as the parallel impedance of the tuned circuit is substantially higher than the two terminals being matched.

Although the same method is sometimes used at the amplifier output, greater matching range is offered through the use of two vari-

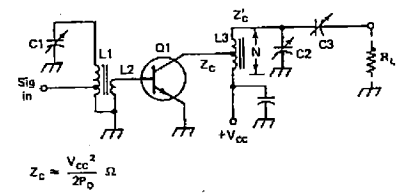



1. $X_{C1} = \dfrac{Z_c}{Q_L} = 49\ \Omega$

2. $X_{C2} = \sqrt{\dfrac{Z_c R_L}{(Q_L^2 + 1) - \dfrac{Z_c}{R_L}}} = 27\ \Omega$

3. $X_{L1} = \dfrac{Q_L Z_c + \left(\dfrac{Z_c R_L}{X_{C2}}\right)}{Q_L^2 + 1} = 67.4\ \Omega$

**Figure 4.7** Pi-network design procedure for bipolar-transistor amplifiers.




$$Z_c \approx \frac{V_{cc}^2}{2P_o}\ \Omega$$

For N:1 turns ratio

1. $X_{L3} = \dfrac{Z_c'}{Q_L} = \dfrac{N^2 Z_c}{Q_L}$

2. $X_{C3} = R_L \sqrt{\dfrac{N^2 Z_c}{R_L} - 1}$

3. $X_{C2} = \dfrac{N^2 Z_c}{Q_L} - \dfrac{1}{\left(\dfrac{1}{X_{C3}} - \dfrac{1}{Q_L R_L}\right)}$

**Figure 4.8** A tapped-coil matching network can be used with solid-state power amplifiers. Basic equations are provided here.





able capacitors (*C*2 and *C*3) and a coil tap. *C*3 of Fig. 4.8 will have the greatest effect on matching to $R_L$, but *C*2 will interlock with it sufficiently to require readjustment of both capacitors several times to effect a matched condition. The major limitation of the collector network, as shown, is poor harmonic suppression. This is particularly true when the tap point on *L*3 is near the top of the coil. The lower the tap location, the higher is the inductive reactance in the path of the harmonic currents, and hence the better the suppression. An advantage is, however, that with the collector of *Q*1 tapped down on *L*3, changes in transistor junction capacitance will have a minor effect on the tank-circuit resonance. Equations are included in Fig. 4.8 for determining the required values of $X_L$ and $X_C$.

## 4.3 BROADBAND TRANSFORMERS

Most modern solid-state power amplifiers for use below 150 MHz employ broadband matching transformers. The suppression of harmonic currents is carried out by means of bandpass or low-pass *LC* filters at the amplifier output. Two kinds of transformers are used for impedance matching in broadband amplifiers. *Transmission-line transformers* are often used. They have windings that have a characteristic impedance and function electrically like sections of two-wire transmission line. The other type of transformer in vogue is the *conventional transformer*. There is some controversy about which type of transformer is best in terms of efficiency and high-frequency response, with the transmission-line transformer being favored in that respect. However, in practice we might find it difficult to differentiate between the two types without special measuring equipment. The losses in a conventional transformer, if they are of special concern, are so low that they are not important for most circuit work. Moreover, the conventional transformer offers the advantage of providing a match to almost any normal combination of impedances below approximately 600 Ω. The transmission-line transformer is limited to specific ratios, such as 4 : 1, 9 : 1, and so on.

Broadband transformers that are used below the VHF spectrum are wound on ferromagnetic cores, such as toroids or balun foundations. Ferrite core material is the usual choice, with the initial permeability ($\mu_i$) running from as low as 40 to as much as 2500, with the higher $\mu_i$ being used at VLH. Powdered-iron core material can be used, but does not have the high permeability found in ferrite compounds; hence a given transformer wound on a powdered-iron core would require a much greater number of coil turns than a comparable transformer wound on a ferrite core of the same physical size. The trade-off is, however, a much lower flux density for ferrite, assuming a core of equivalent size to one made from powdered iron. Therefore, a ferrite core of a specified cross-sectional area will saturate more quickly than a

core using powdered iron. Also, powdered iron is better for use in narrow-band tuned circuits above, say, 10 MHz. This is because the coil or tuned-transformer $Q$ will be higher with the powdered-iron materials.

In principle, a broadband transformer covers a wide range of frequencies effectively because the core material plays a significant role at the lower end of the desired spectrum, but gradually "disappears" from the circuit (electrically) as the operating frequency is increased. Most HF-band broadband transformers are wound on ferrite cores that have a $\mu_i$ of 900 or 950, but permeabilities of 40 and 125 are commonly used for wide spectrums that start at approximately 10 MHz and extend upward in frequency. These can be considered useful rule-of-thumb guidelines.

In essence, we must consider the level of power our broadband transformer must handle, the $\mu_i$, and the core losses. Also, the flux density ($B_{op}$) during operation must be within the linear portion of the BH curve.

When transmission-line transformers are used, we must be aware that the length of the transmission line needs to be great enough to provide the required number of turns on the magnetic core used. Conversely, it cannot be so long that it impairs the high-frequency response of the transformer. The line impedance for a transmission-line transformer can be determined by

$$Z_o = \sqrt{R_{in} R_L}$$

where $R_{in}$ and $R_L$ represent the terminal impedances of the transformer in ohms. In any event, the inductive reactance of the windings should be approximately four times the characteristic impedance of the terminals to which the transformer connects. Hence, if the transformer looks into a 10-Ω load, the inductance of the winding will be based on an $X_L$ of 40 Ω. Therefore,

$$L_{\mu H} = \frac{X_L}{\omega}$$

where $X_L$ is in ohms and $\omega = 2\pi f_{(MHz)}$. Thus, if our lowest operating frequency was 2.3 MHz, and the transformer load was 10 Ω (40 Ω $X_L$), the required inductance to satisfy our winding requirement would be 2.89 μH. The routine procedure is to calculate the necessary inductance for the *smallest* winding of the transformer, as outlined previously. This ensures that the larger winding will have ample inductance to satisfy our rule.

### 4.3.1 Conventional Transformers

We can regard the conventional transformer as we might the audio or power transformer. That is, the windings are placed on the core



separately, and the impedance ratio will be the square of the turns ratio. Therefore, if we needed a 16 : 1 impedance transformation, the transformer turns ratio would be 4 : 1.

Figure 4.9 contains a pictorial and schematic representation of a toroidal transformer of the conventional kind. Figure 4.9(a) shows a

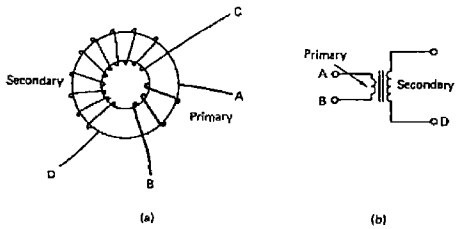



**Figure 4.9** Pictorial and schematic representations of a broadband conventional toroid transformer.

larger winding on the left (secondary) and a small primary winding on the right. The electrical arrangement for this transformer is shown in Fig. 4.9(b). A magnetic-core rod could be used instead of the toroid, with nearly identical performance. The toroid form has the advantage of being self-shielding in nature, which is not true of a similar transformer wound on a rod or flat bar. In a practical situation the large winding would occupy all the core, and the smaller winding would be spread over the larger one. It was drawn as shown to simplify the illustration. Toroidal broadband transformers are most often used in low-level stages of transmitters and in small-signal circuits of other types of equipment.

A more common form of the conventional transformer is seen in Fig. 4.10. It is found in the base and collector circuits of solid-state RF power amplifiers and has the advantage of providing better physical and electrical symmetry than the toroidal style of transformer. In balanced circuits such as push-pull amplifiers, symmetry is important in terms of equal drive to each of the amplifier transistors.

The pictorial views in Fig. 4.10 show two headers ($X$ and $Y$) that are fashioned from circuit-board material. Header $X$ has solid copper on the outer side, to which the brass tubes are soldered to create attachment point $E$, the center tap of the primary winding. Header $Y$ is made the same way, except for a groove down the center that has been etched out of the copper. This isolation groove permits connection points $A$ and $B$ to be electrically isolated from one another. The transformer secondary winding is looped through the copper tubes and exits from

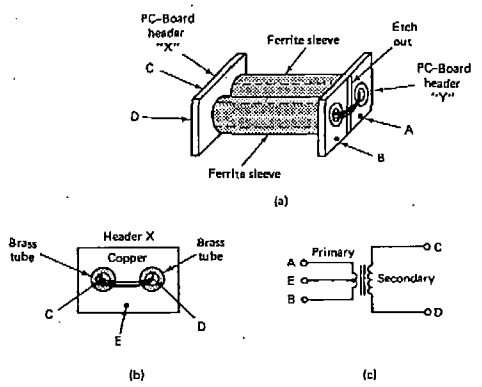



**Figure 4.10** Structural details for a broadband conventional transformer that can be used as a combiner in a balanced circuit.

header $X$. The two lengths of brass or copper tubing constitute the primary winding, which is in effect a U-shaped half-turn. Since this transformer winding is so small, the ferrite material must have a high $\mu_i$ to provide the required winding inductance at the lowest operating frequency. A permeability of 950 is adequate for operation from 2 to 30 MHz in this style of transformer.

It is not imperative to use ferrite sleeves for the circuit of Fig. 4.10. Alternatively, two rows of high-mu toroid cores can be stacked and assembled as shown. The brass tubes and headers will hold them secure, assuming that the tubing fits snugly into the center holes of the toroids.

The transformation ratio is adjusted by adding or substracting turns from transformer winding C-D. Because of the physical character of this style of transformer, it is only possible to obtain even integers when developing a specified turns ratio. This type of broadband transformer lends itself nicely to direct mounting on a printed-circuit board by soldering the headers to the appropriate copper foils on the etched board. A good grade of insulation should be used on the secondary-winding wire, such as Formvar or vinyl. This will help prevent shorted turns on short-circuits to the headers.

### 4.3.2 Transmission-Line Transformers

Transmission-line broadband transformers contain windings that are formed by sections of two-wire transmission line. Often these windings consist of twisted lengths of magnet wire. The pair of wires can be chucked in a hand drill at one end and secured in the jaws of a vise at the opposite end. The drill is operated until the pair of wires has between six and ten twists per inch (25.4 mm). The characteristic impedance of the twisted pair will depend largely upon the wire gauge used. These bifilar windings need not be twisted, but can be laid on the transformer core as parallel conductors. The characteristic impedance will be approximately the same as for the twisted configuration. However, the twisted line is much easier to work with, and it will maintain its impedance more closely over its entire length than will a parallel-pair line, especially if small diameter wire is used.



If we were to construct a parallel-conductor bifilar winding of two lengths of number 30 (AWG) enameled wire, the resultant impedance of the line would be 32 Ω, as discussed by H. O. Granberg in *Electronic Design* for July 19, 1980. An identical pair of number 32 wires would provide a $Z_o$ (characteristic impedance) of 62 Ω. This illustrates the relationship between conductor diameter and $X_o$. We could lower the impedance by twisting two or more pairs of wire together. To illustrate this let us assume we have wound four pairs of number 36 AWG together. The $Z_o$ would now become approximately 18 Ω.

Most transmission-line transformers contain 25-Ω windings. For this purpose we can use subminiature 25-Ω coaxial cable such as Microdot 260-4118-000. Alternatively, two equal lengths of miniature 50-Ω line, such as RG-174/U, when placed in parallel, will yield a 25-Ω $Z_o$. The main limitation in using coaxial cable for the transformer windings is one of physical accommodation. Coaxial lines require larger core sizes than are needed for twisted or parallel sections of magnet wire.

Figure 4.11 shows how a 4 : 1 broadband transformer can be made from two baluns (balanced to unbalanced) to provide superb bandwidth (1.0 to 30.0+ MHz) and high-power capability. There are 14 turns of 25-Ω coaxial cable on each toroid core, but only 3½ turns are shown in order to simplify the illustration. External capacitors can be added to the input and output ports of the transformer to compensate for the leakage inductance. Trimmer capacitors are suggested for C1 and C2 of Fig. 4.12 to permit easy adjustment during the initial test period. Fixed-value capacitors can be substituted later to simplify production of large numbers of the transformers if they are to be used in a manufactured product.

If we analyze the circuit of Figs. 4.11 and 4.12, it will be apparent that the shield braid of the coax cable carries the high current of the low-impedance winding. This contributes to the overall efficiency of the transformer. For the frequency range this transformer accommodates we can use toroids of 950 $\mu_i$, such as Micrometals type 43 of Indiana General Q1. Determination of the correct core size will be discussed later in the chapter.

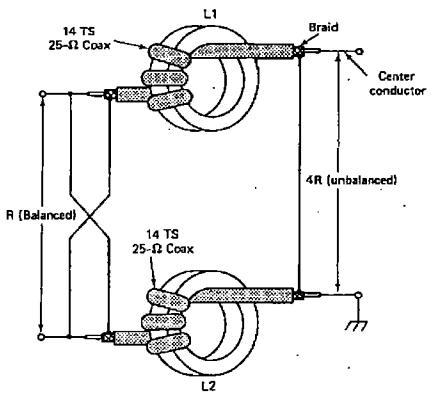



Figure 4.11 Transmission-line transformer technique suggested by Motorola Semiconductor Corp. for using miniature 25-Ω coaxial line sections. A 4 : 1 transformer is shown.

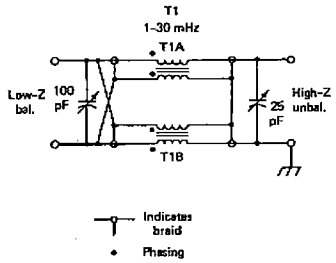



Figure 4.12 Electrical equivalent of the transformer shown pictorially in Fig. 4.11. Input and output trimmers are included for leakage inductance, an aid to high-frequency response. (M. F. "Doug" DeMaw, *Ferromagnetic-Core Design and Application Handbook*, ©1981, p. 101. Reprinted by permission of Prentice-Hall, Inc., Englewood Cliffs, N.J.)

Four classic examples of transmission-line transformers are given in Fig. 4.13. Bifilar windings are used on the cores of all four transformers. Compensating capacitors may be required (as in Fig. 4.12) to extend the high-frequency response.

Additional configurations for broadband transmission-line transformers are suggested in Fig. 4.14. In Fig. 4.14(a) and (b) we find



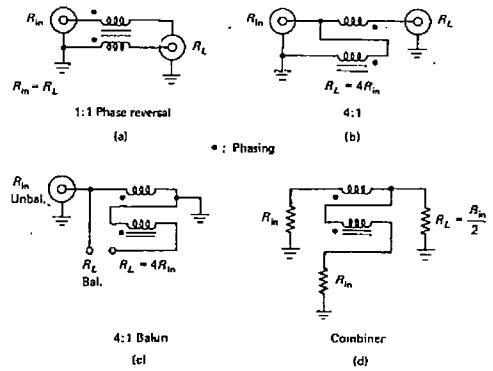



Figure 4.13 Circuit examples of various broadband transformers.

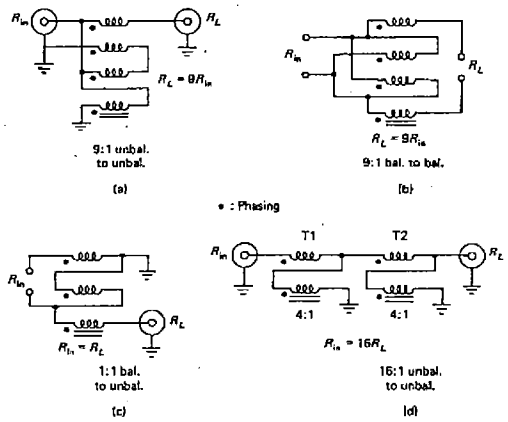



Figure 4.14 Transmission-line transformers that provide various impedance transformations. The windings are bifilar, trifilar, or quadrifilar, as indicated. (M. F. "Doug" DeMaw, *Ferromagnetic-Core Design and Application*, © 1981, p. 102. Reprinted by permission of Prentice-Hall, Inc., Englewood Cliffs, N.J.)

quadrifilar windings. A trifilar style of transformer is seen in Fig. 4.14(c), and cascaded bifilar-wound 4 : 1 baluns are used in Fig. 4.14(d) to provide a 16 : 1 transformation ratio. The specific integers offered by these transformers may not give us a perfect VSWR between the source and load, or amplifier output and $R_L$, but the slight mismatch is seldom a major concern in RF power amplifier design. When better resolution of matching capability is desired, we can employ the transformer shown in Fig. 4.15. It was developed by J. Sevick of Bell Laboratories. Additional $X$, $Y$, and $Z$ taps can be added to the windings to secure ratios as low as 1.5 : 1. If a toroid core with a 2.5 in. (64-mm) diameter is used (125 $\mu_i$ for HF-band use) with number 14 or larger conductor size, the transformer should be capable of handling 1000 W of RF power safely, provided the VSWR on the line is kept below 1.5 : 1. This assumes that the terminal impedances seen by the transformer are quite low, say, 50 Ω or less at each port. A ten-turn quadrifiliar winding on a 125 $\mu_i$ core will be suitable for operation from 2 to 30 MHz.

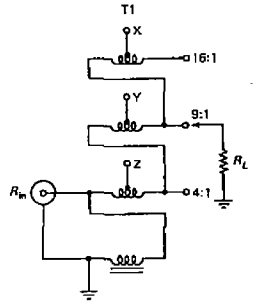



**Figure 4.15** Hybrid type of broadband transformer for matching a variety of common impedances. This design was done by J. Sevick of Bell Laboratories. (M.F. "Doug" DeMaw, *Ferromagnetic-Core Design and Application Handbook*, ©1981, p. 112. Reprinted by permission of Prentice-Hall, Inc., Englewood Cliffs, N.J.)

### 4.3.3 Printed-Circuit Transformers

Broadband and narrow-band transformers can be fabricated on copper-clad circuit board for use at HF and higher. In narrow-band applications the desired amount of inductance and the required transformations can be realized easily by forming the conductors through the etching process. If broadband operation is sought, flat slabs of ferrite can be placed on each side of the etched board and cemented in place. An advantage in this technique is that the compensating capacitors can also be etched on the circuit board. Production cost and time



can be enhanced measurably by utilizing this method. Also, predictable results can be had from a production run once the prototype circuit board has been found acceptable. A simplified illustration of a broadband etched-circuit transformer is given in Fig. 4.16(a). Plates B and C contain the etched inductors of the transformer. In practice, the circuit-board foils would constitute several coil turns rather than the one-turn inductor of B and the two-turn example on board C. Double-sided pc board is used for plates B and C. This permits the large copper tabs of Fig. 4.16 to form compensating capacitors ($C1$ and $C2$) with the ground foil of each board.

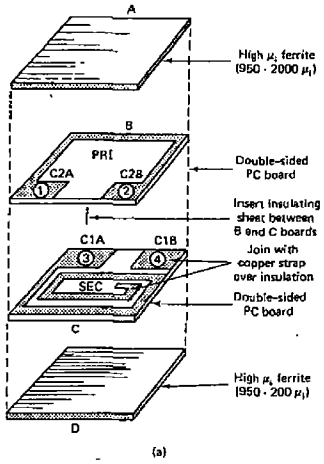



**Figure 4.16** (a) Details for developing broadband transformers with etched circuit boards and ferrite slabs; (b) the electrical equivalent.

The inner coil end of plate C is joined to *C2B* by means of a copper strap that has been soldered to the inductor and the tab. A thin strip of insulating material must be placed between the strap and the inductor to prevent short-circuiting. Finally, the end plates (A and D) are added to form a sandwich of all four pieces. Transformers that are built in this manner are not capable of handling large amounts of RF power, and are limited generally to use in the 10-W or lower power class. An increase in power capability could be realized if the pc boards used Teflon dielectric, and if Teflon sheets were placed between plates A, B, C, and D as insulating elements. The cost of such a technique would probably negate the virtues of this kind of transformer.

#### 4.3.4 Hybrid Transformers

Hybrid transformers are commonly used as power splitters and combiners in solid-state amplifiers. Splitters are used to divide equally the power from a single source and apply it to a load pair, such as splitting a 4-W exciter output and applying the energy to the bases of the transistors in a pair of single-ended amplifiers. In this case there would be approximately 2 W of power delivered to each transistor base.

The combiner transformer is employed at the output of a pair of single-ended amplifiers to combine their powers and deliver the sum to a single load. We can see from this that hybrid transformers can be used for either purpose by simply reversing them to accommodate the application. The energy that is split or summed is of the same phase rather than being of 180° phase difference, as would be the situation if we used center-tapped transformers at the input and output of a push-pull amplifier. Isolation between the ports of a hybrid transformer is on the order of 30 to 40 dB for a properly constructed and applied unit, assuming we are operating from 1.5 to 30 MHz. The isolation effect allows an amplifier to continue operating even though one of the power sources may fail. Of course, failure of one of the amplifiers will result in reduced output power, but a constant load impedance will remain to protect the transistors from damage. Furthermore, the linearity of the amplifier will be maintained. Figure 4.17(a) illustrates how we would connect a hybrid combiner to a pair of amplifiers. *T1* serves as a phase-reversal transformer for feeding $V_{CC}$ to the collectors of the transistors. *T2* is a combiner transformer that delivers the output of the amplifiers to a single-ended load. Both transformers are bifilar wound on ferrite toroid cores of suitable cross-sectional area. For illustrative purposes we have chosen a 15-Ω collector characteristic for each transistor. These two impedances are combined by *T2* and present a 7.5-Ω terminal to the load. *R1* of Fig. 4.17(a) absorbs power when there is imbalance in the amplifier output. It should be rated to handle 0.25 of the power output from the total system.



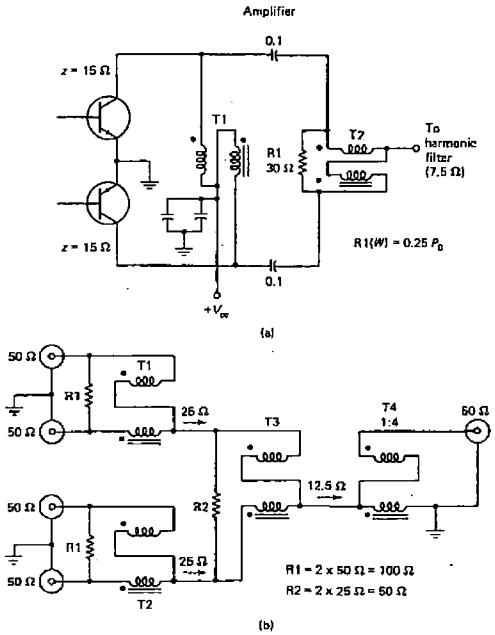



**Figure 4.17** (a) A phase-inverting collector choke (*T1*) in combination with a hybrid combiner (*T2*); (b) a complex hybrid combiner using four broadband transformers. (M. F. "Doug" DeMaw, *Ferro-Magnetic-Core Design and Application Handbook.* © 1981, p. 108. Reprinted by permission of Prentice-Hall, Inc., Englewood Cliffs, N.J.)

The circuit of Fig. 4.17(b) is a complex hybrid combiner that contains four broadband toroidal transformers. *R1* and *R2* are balancing resistors to keep the VSWR at a low value, even if one of the amplifiers fails. Each resistor is twice the ohmic value of the driving source. As in the circuit of Fig. 4.17(a), each resistor should be rated for at least 0.25 of the system output power. The resistors are necessarily of the noninductive type. This general subject was treated in depth by H. Granberg in Motorola's *AN-749* application note.

that reason. A doubly balanced active or passive mixer is the usual choice of the designer in the interest of minimum spurious responses and good dynamic range. Information on mixer design and performance is given in Chapter 6.

Output from the mixer at $f1 + f2$ or $f2 - f1$ is routed through a broadband transformer to a set of switchable $LC$ bandpass filters. They will remove most of the unwanted mixer output frequencies and contribute to purity of the waveform developed by the overall heterodyne generator.

$Q2$ is shown as a Pierce oscillator for use with fundamental crystals below approximately 20 MHz. For higher orders of IF output from the mixer, we could make $Q2$ an overtone type of oscillator to permit using much higher $Q2$ injection frequencies at the mixer, $Q3$. For example, suppose we were interested in extracting a tunable IF of 48 to 50 MHz from $Q3$. Assume that $Q2$ is an overtone oscillator that permits the crystal to oscillate on its third overtone. If we design the VFO to cover a 2-MHz range, we will be able to provide an IF of 48 to 50 MHz by selecting the correct crystal frequency at $Y1$. We will use the sum frequency of the two signal sources, so we will design the VFO to tune from 5 to 7 MHz. Therefore, $Y1$ will have to provide output from $Q2$ on 43 MHz. Thus, $5 + 43 = 48$ MHz, and $7 + 43 = 50$ MHz.

We can take a different approach in our design to cover the same IF range. Four third-overtone crystals could be employed at $Q2$ to yield four 500-kHz switchable IF tuning ranges. If we adopted this technique, it would be necessary for the VFO to tune only 500 kHz rather than 2 MHz. It would also provide much greater bandspread on an analog frequency-readout dial. This technique is the preferred one for many commercial receivers and transmitters operating in the high-frequency spectrum.

Mechanical switching ($S1A$, $S1B$ and $S1C$) can be replaced by diode switching to simplify the mechanical layout of the equipment. A phase-locked loop (PLL) would be a good substitute for the VFO shown in Fig. 5.7, as it would offer improved frequency stability. We can see from the foregoing that the circuit shown is indeed basic and quite flexible with regard to design philosophy. It was used merely to demonstrate the principles of heterodyne frequency generation.

# 6

# MIXERS, BALANCED MODULATORS AND DETECTORS

There is little difference between the functions of mixers, balanced modulators, and detectors in standard communications circuits. All three operate on the principle of combining two frequencies to produce a third one. The design goals are, therefore, quite similar. We are interested in having any of the three circuits perform with high dynamic range, minimum distortion, and good suppression or isolation between the various ports of the circuit device.

We have a number of choices open to us when choosing a particular mixer, modulator, or detector, and the best circuit for the application will be founded on cost effectiveness, performance standards, and available circuit space in the composite product. In all examples we can expect optimum performance from balanced circuits as opposed to single-ended circuits. We need to make a choice between passive and active versions of the three types of circuits, since passive devices yield a conversion loss, and active circuits usually ensure a conversion gain. It should be said, however, that an active mixer, modulator, or detector can exhibit unity gain, or even a conversion loss. This will depend upon how the device is used in the circuit, as we will learn later in the chapter. Figure 6.1 provides a relative comparison between the three circuits we shall examine in this discussion.

## 6.1. MIXERS

The most common use of mixers is found in receivers and heterodyne-frequency generators in transmitters. We have our choice between

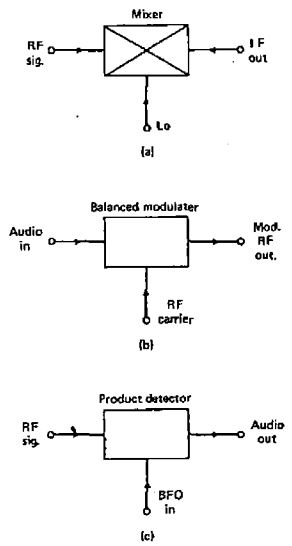



Figure 6.1 Comparison of a mixer, balanced modulator, and product detector.

passive (no operating voltage required) and active (operating voltage needed) devices. Furthermore, we can elect to use the most fundamental form of mixer, the single-ended variety, if high performance is not mandatory, and when equipment cost must be held within specified constraints. The simplest passive mixer is one that contains a single diode. Circuits of this type are sometimes used in UHF and microwave receivers, but are not attractive in circuits that operate below approximately 450 MHz. In the lower VHF region and at high and medium frequencies, it is more desirable to use two diodes in a singly balanced configuration or four diodes in a doubly balanced mixer (DBM). In all instances there will be a conversion loss that is usually of the order of -5 to -8 dB. Additionally, diode passive mixers require substantially greater local-oscillator (LO) power levels to provide the required amount of LO injection to the mixer, as referenced to an active mixer.

Objectively, we want the mixer to withstand strong applied RF signals without creating excessive distortion products. It should also be able to accommodate strong signals without producing cross-modulation effects and gain compression. Gain compression is the point at which a 1-dB reduction in mixer output occurs when the RF input signal level is increased until that value of compression takes place.



Another important consideration is the mixer noise figure (NF). This is especially important above, say, 15 MHz, where the atmospheric noise is often lower in amplitude than is the receiver front-end noise. Mixers are much noisier in mixer service than they are as RF amplifiers when the same device is used in each application. When the mixer noise becomes too great for the operating frequency, we can reduce the effective receiver NF by using a low-noise RF amplifier ahead of the mixer. Its gain must exceed that of the mixer if an improvement is to be realized. Also, the local oscillator and its associated amplifiers must be as spectrally pure as possible in terms of noise before the LO energy is injected into the mixer. Excessive noise output from the LO system will effectively increase the mixer noise figure. Eliminating this noise is an important design problem if we are to strive for high receiver performance. The penalty for using a preamplifier is observed in reduced mixer dynamic range, owing to the increased RF signal level that is applied to the mixer input port. It can be seen from this discussion that all manner of design trade-offs accompany the implementation of a mixer.

Still another important mixer parameter is the intermodulation distortion (IMD) products generated within the device. The IMD should be as low as possible to ensure high dynamic range. IMD is manifested as additional unwanted receiver responses to one or more strong signals in the receiver passband. The effect is one of having a single incoming signal appear in several places as the receiver is tuned away from the signal that is causing the IMD responses. The IMD products are numerically related to the interfering signal and another strong signal nearby in the receiver passband. The IMD characteristics of a given mixer can be determined in laboratory tests by applying two RF signals at the mixer input (two-tone test) and observing the third-order distortion products at the mixer output. A block diagram of a suitable setup for mixer evaluation is shown in Fig. 6.2. A spectrum analyzer, two signal sources, a LO source, step attenuators, a combiner, and post-mixer amplifier and lattice filter are required. The post-mixer amplifier must be as good as or better than the mixer under test (MUT) in terms of IMD. A CATV bipolar transistor (2N5109) meets the requirement easily when operated in a linear broadband configuration.

Port-to-port signal isolation is a vital mixer consideration. That is, we do not want the LO energy to appear at the RF or IF ports of a mixer in sufficient magnitude to create additional frequencies through unwanted mixing action. Doubly balanced mixers offer the best solution to port isolation. Singly balanced mixers are the second choice, and single-ended mixers are the worst we might select for resolving the problem.

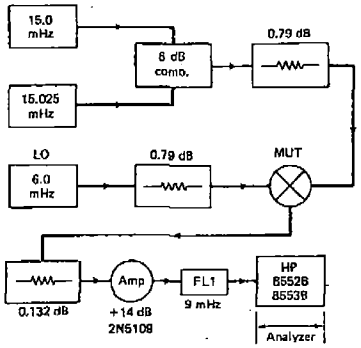



Figure 6.2 Block diagram showing the test setup for measuring mixer dynamic range.

Maximum mixer conversion gain will occur only when the input and output of the mixer are well matched to the characteristic impedances of the source and load. Intentional mismatch is often applied to reduce the conversion gain and to enhance the IMD characteristics by operating the output of an active mixer at low impedance levels. This technique reduces the ac voltage swing and helps to keep the collector or drain of a mixer transistor within a more linear operating range.

### 6.1.1 Single-Ended Mixers

The practicality of active single-ended mixers is realized in the design of inexpensive receivers, such as the pocket-sized AM band transistor radio. A bipolar-transistor mixer is capable of delivering conversion gains as great as 30 dB under well-matched conditions and careful biasing. Unfortunately, the dynamic range of such a mixer is very poor, which helps to explain the unsatisfactory strong-signal performance of most imported "pocket radios." But this type of mixer contributes to a reduction in receiver stages with respect to overall receiver gain. RF amplifiers are seldom used in receivers of this general variety.

Figure 6.3 contains the circuit of a typical single-ended bipolar mixer. Approximate values are listed for the components and operating voltages for best performance. A mixer is necessarily a nonlinear device and would operate, ideally, with a square-law response. Therefore, the



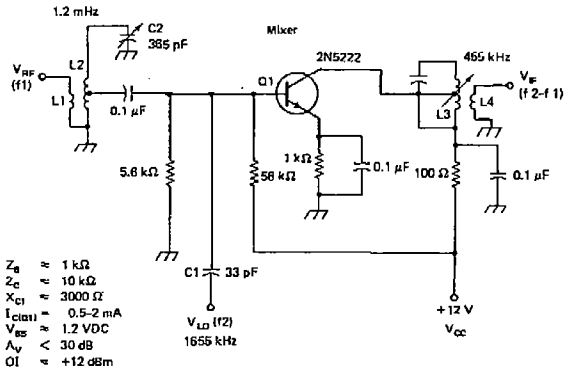



Figure 6.3 Practical circuit for a bipolar-transistor mixer.

forward bias on Q1 of Fig. 6.3 is held to a low value. The $V_{BB}$ used will aid conversion gain and enhance the weak-signal response of the mixer. The base of Q1 is tapped toward the grounded end of L2 to effect an impedance match between the mixer input and the antenna. Typically, the input impedance of this kind of mixer is 1000 Ω.

The collector could be connected directly to the top end of L3, since the characteristic impedance of the collector will be on the order of 10,000 Ω with the biasing specified in Fig. 6.3. By tapping the collector down on the tuned circuit we can control the conversion gain (reduce it) to a desired value. Also, as the collector is tapped down on the tuned circuit, we are minimizing the loading effects on the tuned circuit, thereby elevating the Q. This provides increased selectivity at the mixer output. This mixer requires very low injection power from the LO. Since we are applying 0.5 V rms of LO signal across the base-emitter port, the power requirements will be minimal. C1 should have fairly high reactance at the signal frequency to prevent undue loading of the input tuned circuit by the LO circuitry. Light coupling via C1 will also help reduce oscillator pulling when C2 is adjusted.

Mixer distortion (IMD) can be defined either in terms of the IMD products being a specified number of decibels below the desired output signal level (IF) or by means of the third-order output intercept number. The intercept point is an imaginary point established when a 10-dB increase in the two input test tones causes the desired mixer output

products to increase by 10 dB, but the third-order IMD products increase by 30 dB. In other words, if we had a mixer that was without a gain-compression trait, we could find a point at which the level of the desired output product would be equivalent to that of the third-order IMD product. We would define this as the third-order intercept point, the position on a set of curves where the desired output-product curve intersected with the curve of the third-order product. This is shown in Fig. 6.4. The curves in this hypothetical example converge at the +20

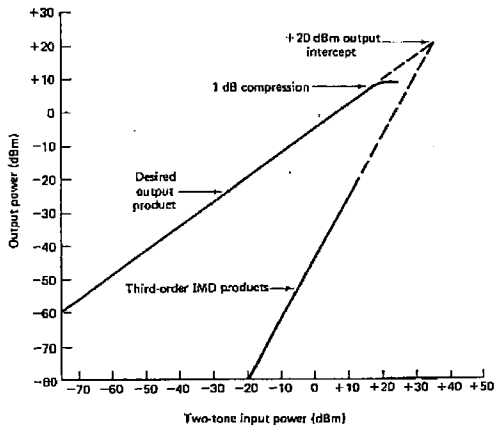



**Figure 6.4** Curves that show the third-order output intercept point of a mixer.

dBm output intercept point. It becomes apparent that the greater the output intercept number, the higher is the dynamic range of the mixer. In the case of the circuit of Fig. 6.3 the output intercept is quite low, +12 dBm. Strong mixers yield numbers as great as +45 dBm. A typical number for a medium-quality receiver would be on the order of +25 dBm.

In terms of mixer performance our concern is for the third-order *input intercept* characteristic, even though it is related directly to the output intercept number. The input intercept can be obtained by subtracting the conversion gain of the mixer from the output. Hence, if the conversion gain were 10 dB and the output intercept were +35 dBm,



the input intercept would be +25 dBm. It can be seen from this that it is important to minimize the mixer conversion gain in the interest of elevating the input-intercept characteristic. Frequently, this is done in an active mixer by using broadband techniques and introducing intentional mismatches at the input and output ports. Irrespective of the mixer input intercept, the final determination of receiver performance is based on the *receiver input intercept* number. This dictates that care must be given to the design of the input circuitry, inclusive of the RF amplifier that precedes the mixer, in the event that such a stage is used.

A JFET is capable of better performance in a single-ended mixer, compared to a bipolar transistor. Figure 6.5 illustrates how we might

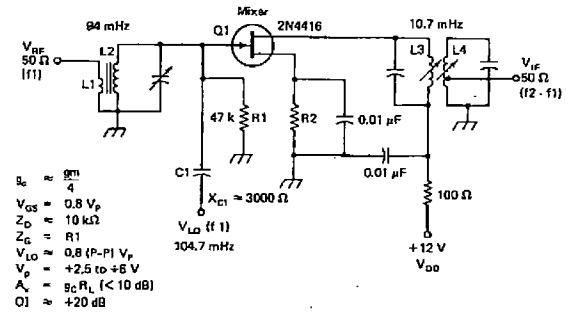



**Figure 6.5** Practical JFET single-ended mixer.

use a 2N4416 or similar FET as a mixer. Conversion transconductance ($g_c$) will be approximately 0.25 the $g_m$ of the same device in amplifier service. Hence, if the FET was rated at 5000 μS as an amplifier, the conversion transconductance would be roughly equal to 5000/4, or 1250 μS. Once we know this number we can approximate the conversion gain by

$$A_V = g_c R_L$$

where $A_V$ is the voltage gain in decibels, $g_c$ is the conversion transconductance in siemens, and $R_L$ is the drain load in ohms. Therefore, if we had a 1250 μS (0.0125 S) $g_c$ and an effective mixer drain load of 1000 Ω, the gain would be

$$A_V = 0.0125 \times 1000 = 12.5 \text{ dB}$$

We will impair mixer performance, however, if we attempt to elevate the conversion gain by increasing the drain load impedance. In the

circuit of Fig. 6.5 we would be prudent to tap the FET drain toward the $V_{DD}$ end of $L3$ to force the drain down to a lower impedance than it sees in the circuit, as shown. Typically, the drain impedance will be approximately 10 kΩ with a circuit such as that of Fig. 6.5. This technique will reduce the peak drain-voltage swing, thereby reducing the change in junction capacitance. The latter, which introduces a *varactor effect*, results in the generation of harmonic currents.

Source resistor $R2$ is selected to yield a gate-source dc potential that is 0.8 the pinchoff voltage ($V_p$) of the FET. In practice, this will be a somewhat arbitrary number, as the manufacturers' data sheets are not specific. $V_p$ is not listed in most of the literature, but we can use the more common parameter, $V_{GS(off)}$, which is of equal magnitude to $V_p$, but of opposite polarity. For a 2N4416 the spread is listed as -2.5 to -6 V, equating to a $V_p$ of +2.5 to +6 V. Arbitrarily, we can assume a midrange value for $V_p$, accepting in our design example a voltage of 4.25. Therefore, $R2$ will be chosen to yield a $V_{GS}$ of 0.8 × 4.25, or 3.4 V. Because the listed $V_{GS(off)}$ values are rather nebulous, we will fare much better in the final analysis by making empirical adjustments to the $V_{GS}$ while the mixer is in operation. A compromise between IMD and conversion gain must be made when establishing the operating conditions. Ideally, the $g_c$ should be held below 10 dB in the interest of good mixer performance.

Under the foregoing guidelines the LO injection should be approximately 0.8 p-p the $V_p$ value. An output intercept of +20 dBm is typical for the mixer of Fig. 6.5, although a theoretical value of +30 dBm exists for FETs such as the U310 in a fully optimized circuit. Since gate injection of the LO is suggested in our circuit example, $C1$ should follow the rule set forth for the circuit in Fig. 6.3. Source injection can be used in this style of circuit, but substantially more LO power will be required and mixer instability may result.

Dual-gate MOSFETs provide comparable performance to JFETs in mixer circuits. They offer the advantage of having a pair of gates rather than a single gate, thus making it easy to introduce the LO and RF signals at separate ports. Normally, the LO energy is applied to gate 2 and the RF input signal is routed to gate 1, as demonstrated in Fig. 6.6. This type of FET is rather fragile in terms of excessive gate voltage, compared to a JFET, but the isolation between the two gates is advantageous toward minimizing LO pulling effects and interaction between the LO output circuitry and the RF signal input circuit. Some manufacturers rate the gate-to-gate isolation as high as 50 dB, but in a practical circuit that magnitude of signal separation would be difficult to achieve. A 25- to 30-dB isolation value is more common, owing to stray coupling external to the MOSFET.

Gate 2 can be biased separately by means of a resistive voltage divider connected to the $V_{DD}$ line. Comparable performance can be ob-



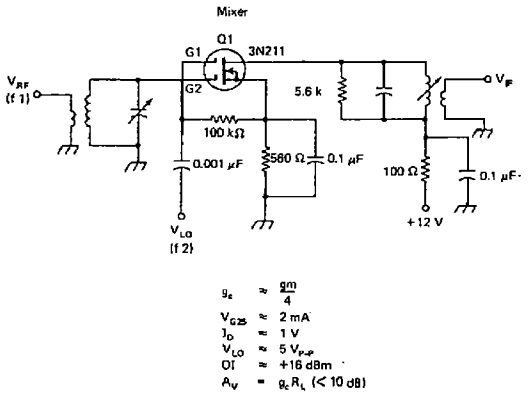



**Figure 6.6** Improved single-ended mixer performance can be realized by using a dual-gate MOSFET, which permits two-port injection.

tained, however, by strapping gate 2 to the source through a 100-kΩ resistor, as seen in Fig. 6.6. With a 560-Ω source-bias resistor, an effective gate 2 potential of 1 V will result. Under these conditions, a peak-to-peak LO injection of 5 V will enable the mixer to have reasonable conversion gain and acceptable IMD characteristics. Optimum third-order output intercept for a 3N211 was noted during laboratory tests when $V_{g2s}$ was set at 4.2 V, and with an 8-V p-p LO injection level. This resulted in a third-order output intercept of +16 dBm. Lowering the drain load impedance of Q1 in Fig. 6.6 would have aided the output intercept number. The 5.6 kΩ resistor across the output tuned circuit pulls the drain down to an impedance that yields better IMD performance. In a test circuit that contained two 3N211 transistors in a singly balanced mixer, and with broadband coupling transformers at the input and output of the mixer, a third-order output intercept of +20 dBm was observed. The gates and drains were operated at a 200-Ω impedance. Conversion gain was approximately 6 dB when 4.2 V of $V_{g2s}$ was applied, and with an 8-V p-p LO injection level. A 560-Ω resistor was used in each source return.

### 6.1.2 Balanced Mixers

Balanced mixers offer better port-to-port signal isolation than is possible with single-ended mixers. A comparison of the output products

from single-ended, singly balanced and doubly balanced mixers is presented in Table 6.1. It becomes immediately apparent that the doubly

TABLE 6.1 Comparison of Output Products from Mixers

| (N) | Single-Ended Mixer | | | | |
|---|---|---|---|---|---|
| | $f_o$ | $2f_o$ | $3f_o$ | $4f_o$ | $5f_o$ |
| $f_s$ | $f_o \pm f_s$ | $2f_o \pm f_s$ | $3f_o \pm f_s$ | $4f_o \pm f_s$ | $5f_o \pm f_s$ |
| $2f_s$ | $2f_s \pm f_o$ | $2f_o \pm 2f_s$ | $3f_o \pm 2f_s$ | $4f_o \pm 2f_s$ | $5f_o \pm 2f_s$ |
| $3f_s$ | $3f_s \pm f_o$ | $3f_s \pm 3f_o$ | $3f_o \pm 3f_s$ | $4f_o \pm 3f_s$ | $5f_o \pm 3f_s$ |
| $4f_s$ | $4f_s \pm f_o$ | $4f_s \pm 2f_o$ | $4f_s \pm 3f_o$ | $4f_o \pm 4f_s$ | $5f_o \pm 4f_s$ |
| $5f_s$ | $5f_s \pm f_o$ | $5f_s \pm 2f_o$ | $5f_s \pm 3f_o$ | $5f_s \pm 4f_o$ | $5f_o \pm 5f_s$ |
| (0.5 N) | Singly Balanced Mixer | | | | |
| | $f_o$ | $2f_o$ | $3f_o$ | $4f_o$ | $5f_o$ |
| $f_s$ | $f_o \pm f_s$ | $2f_o \pm f_s$ | $3f_o \pm f_s$ | $4f_o \pm f_s$ | $5f_o \pm f_s$ |
| $2f_s$ | — | — | — | — | — |
| $3f_s$ | $3f_s \pm f_o$ | $3f_s \pm 2f_o$ | $3f_s \pm 3f_o$ | $4f_o \pm 3f_s$ | $5f_o \pm 3f_s$ |
| $4f_s$ | — | — | — | — | — |
| $5f_s$ | $5f_s \pm f_o$ | $5f_s \pm 2f_o$ | $5f_s \pm 3f_o$ | $5f_s \pm 4f_o$ | $5f_o \pm 5f_s$ |
| (0.25 N) | Doubly Balanced Mixer | | | | |
| | $f_o$ | $2f_o$ | $3f_o$ | $4f_o$ | $5f_o$ |
| $f_s$ | $f_o \pm f_s$ | — | $3f_o \pm f_s$ | — | $5f_o \pm f_s$ |
| $2f_s$ | — | — | — | — | — |
| $3f_s$ | $3f_s \pm f_o$ | — | $3f_o \pm 3f_s$ | — | $5f_o \pm 3f_s$ |
| $4f_s$ | — | — | — | — | — |
| $5f_s$ | $5f_s \pm f_o$ | — | $5f_s \pm 3f_o$ | — | $5f_o \pm 5f_s$ |

LO = $f_o$, signal frequency = $f_s$
$2f_o \pm f_s$ = third-order product
$3f_s \pm 3f_o$ = sixth-order product, etc.
$N$ = number of mixer products

balanced mixer is the stellar performer in terms of isolation and product suppression. It is, thus, the mixer preferred by designers of high-performance equipment.

An example of properly designed JFET singly balanced mixer is seen in Fig. 6.7. It is similar to a circuit suggested by E. Oxner of Siliconix in *Application Note AN72-1*. Dynamic balance is assured through the use of a U430 dual-FET unit. $R1$ is selected to give a $V_{gs}$ of 0.8 the pinchoff voltage, which will be on the order of 2 V, allowing for the published spread of -1 to -4 V, $V_{gs(off)}$. Symmetrical feed is used at the mixer input by means of $T1$, $T2$, and $T3$, providing a 180° phase dif-



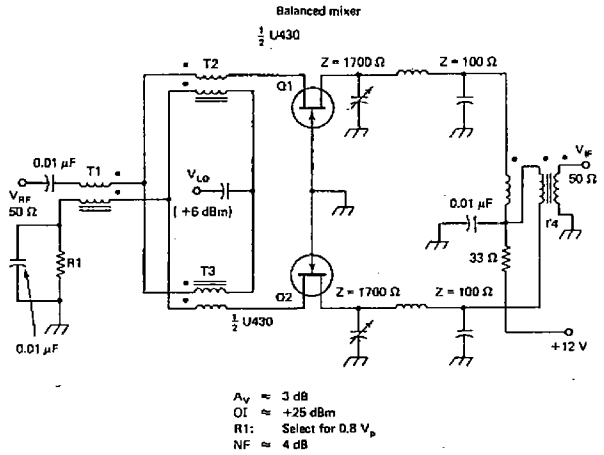



Figure 6.7 Dual FET balanced mixer using a Siliconix U430 device.

ferential between the sources of $Q1$ and $Q2$. The transformers are all wound on 125 $\mu_i$ ferrite toroid cores, 0.37-in. diameter. $T1$, $T2$, and $T3$ contain bifilar windings of 15 turns of number 26 enameled wire. $T4$ is wound on a 0.5-in. diameter ferrite core ($\mu_i$ = 125), trifilar fashion, with 15 turns of number 26 enameled wire. These transformer dimensions are suitable for use from 3 to 30 MHz.

Low-pass matching networks are used in the drains of the FETs to lower the drain impedance to 1700 Ω. They are structured to transform the impedance from 1700 ohms to 100 Ω. The 4 : 1 impedance ratio of $T4$ matches the mixer to a 50-Ω load. Best performance results when $V_{LO}$ is 0.8 p-p $V_{gs(off)}$.

A singly balanced diode mixer is presented in Fig. 6.8. It suffers the same limitations found in singly balanced active mixers, and in addition it yields a conversion loss of approximately 6 to 8 dB. $T1$ is a trifilar-wound toroidal broadband transformer. $T2$ is also a broadband transformer, which is used to provide a step-up transformation to the mixer load. The turns ratio is chosen accordingly. Matched silicon switching diodes are satisfactory in this circuit, but hot-carrier diodes will offer improved performance.

A quad of matched silicon or hot-carrier diodes can be used to

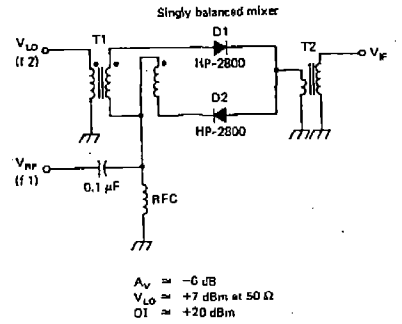



**Figure 6.8** Singly balanced two-diode mixer using broadband transformers.

create a doubly balanced diode-ring mixer of the type shown schematically in Fig. 6.9. The circuit, minus $T1$ and $T4$, is typical of the manufactured DBM mixer modules found on the industrial market. Well-designed mixers of this kind offer excellent broadband characteristics, with effective bandwidths of more than 100 MHz. A typical DBM might be rated from 500 kHz to 500 MHz. Medium-level DBMs require an LO power of approximately +7 dBm, whereas the high-level DBMs call for LO powers of +15 dBm or greater. Conversion loss is comparable to that of the mixer in Fig. 6.8, being roughly 6 dB.

Transformers $T1$ and $T4$ of Fig. 6.9 can be added to serve as baluns. This aids the overall balance of the mixer by maintaining sym-

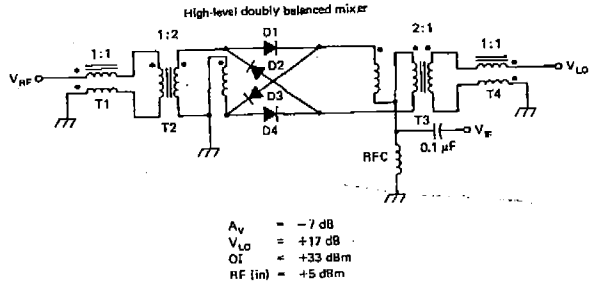



**Figure 6.9** High dynamic range and good port-to-port isolation can be had from a doubly balanced diode-ring mixer.



metry at the input and output ports of the circuitry between the input of $T2$ and the output of $T3$. $T1$ and $T2$ are bifilar wound, and trifilar windings are laid on the cores of $T2$ and $T3$. Output intercept for this type of mixer (high level) is typically +33 dBm. Best performance results when the mixer is terminated in 50 Ω by means of a diplexer.

An example of a diplexed DBM is seen in Fig. 6.10. A high-pass network consisting of $L1$, $C1$, and $C2$ is connected to the IF port of the

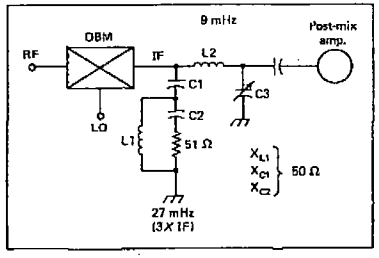



**Figure 6.10** A diplexer can be added to a DBM for the purpose of presenting a 50-Ω termination. This improves mixer IMD.

mixer. It is designed for a cutoff frequency of three times the IF. A $Q_L$ of 1 is satisfactory; hence we can use an $X_L$ and $X_c$ of 51 for the resistive termination of 51 Ω. A simple low-pass $L$ network is used between the IF port of the DBM and the post-mixer amplifier to provide an impedance match to 50 Ω. The transformation ratio will be dependent upon the input impedance of the amplifier that succeeds the mixer. Improvements in mixer IMD of 2 to 4 dB have been observed by the addition of the diplexer.

### 6.1.3 IC Mixers

We could spend countless hours discussing the various types of IC mixers and their respective virtues. Such a treatment is beyond the scope of this text. Therefore, we will examine two of the more common IC mixers for illustrative purposes.

An advantage found in the application of balanced mixers that use ICs is the inherent balance and tracking with temperature that prevails. This is because the bipolar transistors and resistors that are within the IC were all formed at the same time on a common slice of silicon (substrate). This yields transistors with nearly identical dynamic characteristics. Also, when there are temperature excursions of the operating

IC, balance will be maintained through excellent tracking of the component values within the IC package.

A singly balanced IC mixer is depicted in Fig. 6.11(a). It employs an RCA CA3028A IC, which is seen in schematic form in Fig. 6.11(b). The device consists of a differentially arranged pair of *npn* silicon transistors. A third transistor functions as a current source in the emitter returns of the differential pair. This IC offers good mixer performance up to at least 100 MHz. As configured in Fig. 6.11(a), it will provide a conversion gain of about +10 dB with an output intercept of approximately +20 dBm. A broadband transformer is used at the input of the mixer to establish a 180° phase difference at the bases of the differential pair. A tuned transformer is used at the mixer output to provide filtering action and a positive conversion gain. The turns ratio of the tuned transformer is chosen to provide a match between the mixer output and the load. The CA3028A has a base-to-base input impedance of approximately 2000 Ω. The collector-to-collector output impedance is on the order of 8000 Ω.

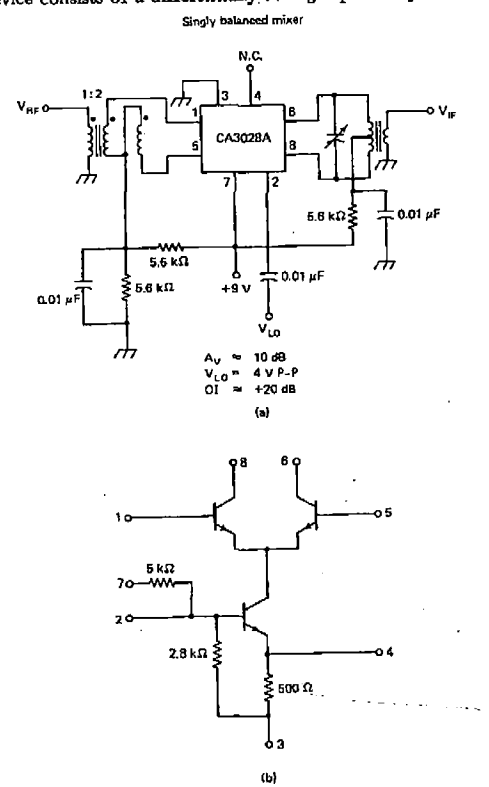



Figure 6.11 CA3028A IC used as a singly balanced mixer; (b) internal circuit of the IC.



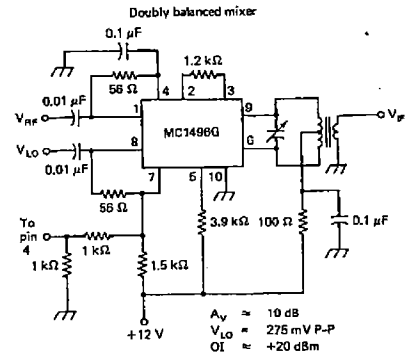
A doubly balanced IC mixer is presented in Fig. 6.12(a). It contains a Motorola MC1496G, which is seen schematically in Fig. 6.12(b). In balanced operation the two differential pairs of *npn* transistors are cross-connected to give a doubly balanced arrangement. Optimum performance will be obtained through experimentation with the biasing values of the circuit. The component values in Fig. 6.12(a) are approximately those suggested by the manufacturer, but the author has seen laboratory reports that indicated improved IMD performance by optimizing the biasing of the IC.

The input and output impedances of the MC1496G are similar to those that characterize the CA3028A of Fig. 6.11. LO suppression at the mixer output is between 40 and 65 dB, depending on the operating frequency and the degree of circuit balance.

### 6.1.4 High-Level Balanced Mixers

In the interest of high orders of mixer dynamic range, we can utilize mixers that are more powerful than those just described. One IC type of mixer chip that has proved effective in this regard is the Plessey SL6440C. Although similar in concept to the MC1496G, it can be programmed to exhibit a third-order output intercept of +31 dBm. The programmable feature entails the controlled flow of current into pin 11 of the IC. Maximum quiescent current in the differential transistors is 50 mA. Total device dissipation at 25°C is 1200 MW maximum.

Figure 6.13 depicts the laboratory test circuit used to evaluate the SL6440C. Broadband balun transformers are used to provide balanced input and output conditions. This arrangement results in a 50-Ω impedance being presented to the input and output ports of the IC. Conversion gain was measured as 0 dB, although the manufacturer rates it at -1 dB. This number was determined with 50-Ω input and output terminations on the IC (desired to lower the $A_V$ and improve the input intercept) and a programmed current ($I_p$) of 35 mA. The author measured the noise figure at a signal frequency of 15 MHz and found it



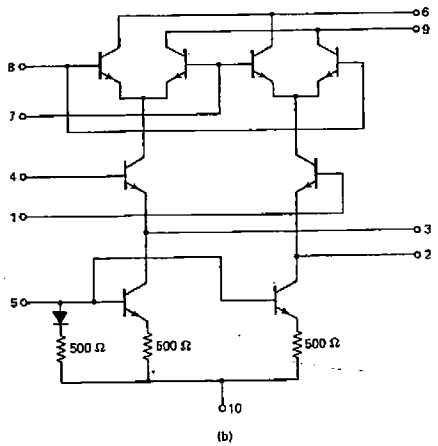




**Figure 6.12** (a) Doubly balanced active mixer with a Motorola MC1496G IC; (b) the inner workings of the chip.



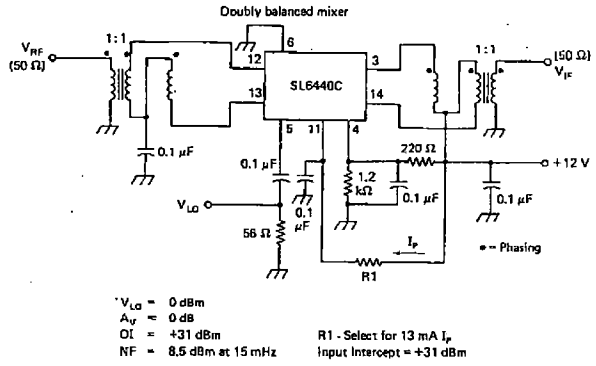



**Figure 6.13** A high-level doubly balanced mixer can be obtained by using the Plessey SL6440C IC. Excellent dynamic range is possible with this circuit.

to be 8.5 dB. Plessey rates it at 11 dB at a signal frequency of 100 MHz, the same frequency at which the -1-dB gain was determined.

In the circuit of Fig. 6.13, $R1$ is chosen to permit the desired value of $I_p$. In the author's tests it was noted that an $I_p$ of 13 mA resulted in optimum mixer performance with an LO level of 0 dBm and an RF signal input of -5 dBm. Under these conditions the LO isolation at the mixer output was 30 dB. The $2f$ LO energy was measured at -75 dB.

If we desire a very strong mixer, we might consider using VMOS power FETs as the active devices. Once again there is the matter of cost-effectiveness to consider, plus the physical bulk of the mixer module. The power FETs are substantially larger than ICs or small-signal devices, and because of the power they dissipate it is necessary to employ heat sinks. Moreover, the power consumption of a VMOS mixer is rather high, placing still another constriction on the design. However, the performance of this variety of mixer offers many advantages, the most significant being high dynamic range if the conversion gain is minimized.

A practical circuit for a high-level, singly balanced VMOS power FET mixer is shown in Fig. 6.14. VHF transistors are used in this laboratory test model, primarily to take advantage of the strip-line packaging format, which lends itself well to heat sinking. Some of the less expensive VMOS units would no doubt yield similar performance, such as the Siliconix VN66AKs, but the TO-5 package would impose restrictions