IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Asad Abidi

1 Background and Qualifications

§1 I am currently a Distinguished Chancellor's Professor of Electrical Engineering at the University of California, Los Angeles ("UCLA"). I have been a professor at UCLA since 1985. Prior to UCLA, I was at Bell Laboratories as a member of their technical staff in the Advanced LSI Development Laboratory. I was also a visiting faculty researcher at Hewlett Packard Laboratories in 1989.

§2 My research interests at present are focused on circuit methods to overcome fundamental limitations on the performance of the radio portions of single-chip wireless receivers and transmitters. I also maintain active research on circuits and architectures for analog-to-digital converters, which includes sample-and-hold circuits.

§3 In 2007, I was elected to the National Academy of Engineering for my contributions to the development of single-chip radios that have enabled the handheld wireless devices of today. This is the highest peer recognition that an engineer receives in the US. A copy of my curriculum vitae, which describes in further detail my qualifications, responsibilities, employment history, honors, awards, professional associations.

2 Information Provided to Me

2.1 Basis

§4 I have reviewed United States Patent No. 7,496,342 ("the '342 patent") to Sorrells *et al.*, Exhibits 1001. I have also read the patent documents and printed publications cited in the endnotes of this declaration.

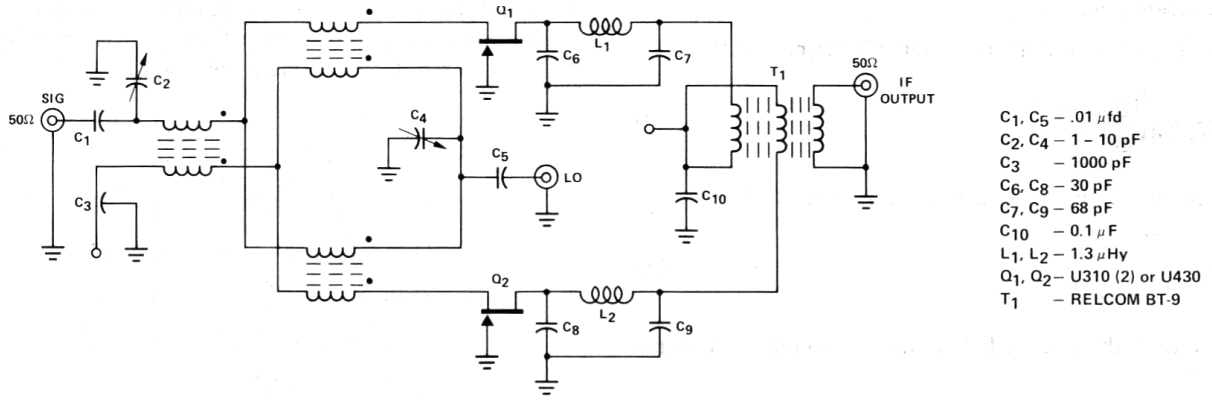
§5 I have been informed by counsel for the petitioner that the level of ordinary skill in the art is evidenced by the references. I have further been informed that the parties in the Qualcomm litigation appear to have generally agreed that one of ordinary skill in the art (sometimes referred to herein as "one skilled in the art") would have "a Bachelor's of Science degree in Electrical Engineering and four years of experience in the wireless communications industry". This is consistent with the level of skill evidenced by the references cited herein.

3 '342 Claims, Prior Art, and Obviousness

Claim 342-18. *A method for downconverting an electromagnetic signal, comprising the steps of:*
(1) receiving an information signal;
(2) inverting the information signal to generate an inverted information signal;
(3) electrically coupling the information signal to a first capacitor and the inverted information signal to a second capacitor;
(4) controlling a charging and discharging cycle of the first and second capacitors with first and second switching devices electrically coupled to the first and second capacitors, respectively; and
(5) performing a plurality of charging and discharging cycles of the first and second capacitors to generate first and second downconverted information signals across first and second impedance devices, respectively;
wherein the information signal is used to store a charge on the first capacitor when the first switching device is closed and the inverted information signal is used to store a charge on the second capacitor when the second switching device is closed.

3.1 Prior Art: Oxner (1979)

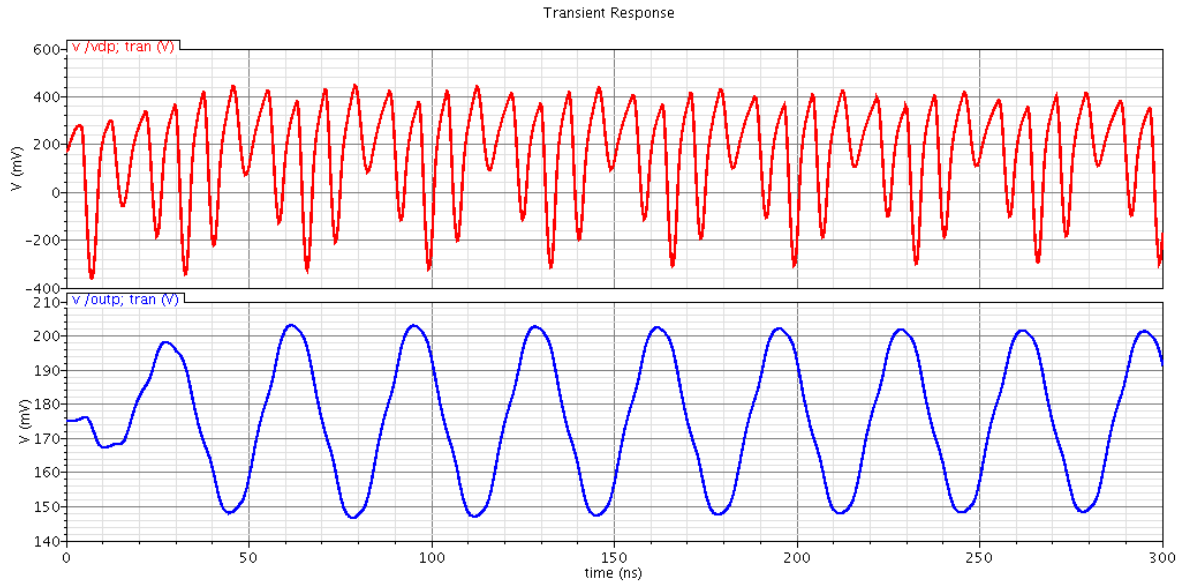
[1] shows a circuit (Fig. 3.1(a)) that receives an information signal at the port labelled "SIG", inverts it in a transformer balun to create a balanced signal (in-phase and anti-phase), and couples the in-phase signal to a first capacitor C6 and the anti-phase to second capacitor C8 through switching devices JFETs Q1 and Q2. A large local oscillator (LO) sinewave is added to each SIG input through two other transformers. The LO signal, which in typical use will be much larger than the SIG input signal, will turn the JFETs Q1 and Q2 ON and OFF. The n-channel JFETs will turn OFF when the source terminal voltage is typically +1V [2]. These capacitors are charged and discharged through Q1 and Q2 by the bidirectional current flow that is determined by modulation in the incoming information signal. Each capacitor stores a charge as a result of the attached switch being turned on. C6, L1 and C8 form a lowpass filter, as do C7, L2, and C9, that suppresses the LO and RF frequencies and passes to its output (the voltages across C8 and C9) substantialy the waveform at IF. This waveform is combined in



Prototype Active Balanced Mixer

Figure 2

(a)



(b)

Figure 3.1: Oxner's Mixer: (a) Circuit, (b) Simulated voltages across C_6 and C_7.

T1 and delivered to the 50 ohm load at the output of Oxner's circuit. The output transformer (T1) converts balanced signals to single-ended[1], rejecting any LO signal at the output. Thus, although this circuit downconverts by sampling the SIG input, it has the LO rejection property of a conventional double-balanced mixer. The spectrum of the IF Output lies at the difference frequency between the SIG input and the LO.

Fig. 3.1(b) shows the simulated waveforms of voltages on C6 and C8.

3.2 Obviousness of Symmetric, Balanced Circuits

§6 Anyone ordinarily skilled in the art would have known the benefits of symmetric balanced versions of single-ended circuits. For example, when a balanced circuit is driven differentially and sensed differentially at the output, it will reject common-mode disturbances and it will null even-order distortion. Systematic methods were well-known on how to construct a symmetric circuit starting from a single-ended circuit; see [4, Sec. 6.3], for example, on how to construct a balanced amplifier starting from a single-ended amplifier, and [5] on how to develop a four-quadrant analog multiplier[2] with two differential inputs and a differential output, starting from a prototype multiplying circuit with single-ended inputs and output. The advantages of balanced mixers in rejecting a large LO signal have been known for a very long time. [6, Fig. 4.20] describes several transformer-based balanced modulators that use diodes. [7] is the original disclosure of an all-transistor balanced modulator.

Loop and dipole antennas by their very nature supply a differential output, so they require no separate means for signal inversion [3]. Otherwise transformer baluns were well known to all practitioners as an apparatus that transforms a single-ended signal into a balanced differential signal, e.g. [3, Fig. 10.13(b)].

3.3 Prior Art through Obviousness

§7 It would be obvious to use a differential version of Fig. 82B of the '551 patent, with a balun at the input, to fulfill all the steps of Claim 18.

§8 It would be an obvious extension of the single-ended sampling mixer shown in [8, Fig. 14] to create a balanced version that fulfills all parts of Claim 18. [8, Sec. 5.5] shows one step towards a fully differential realization. [6, Fig. 4.20] serves as a guide to double balanced modulators that use diodes.

3.4 Discussion

[1] This is often a two-winding transformer, where one winding is tapped at its center and connected to a fixed potential [3, Fig. 10.13(b)]. The balanced signal is applied to the free terminals of this winding. In [1, Fig. 2] this center tap connects to decoupling capacitor C_{10} and a bias voltage. The other winding responds to differential signals applied to the first winding, but rejects common-mode signals.

[2] A four quadrant analog multiplier is commonly used as a double-balanced mixer.

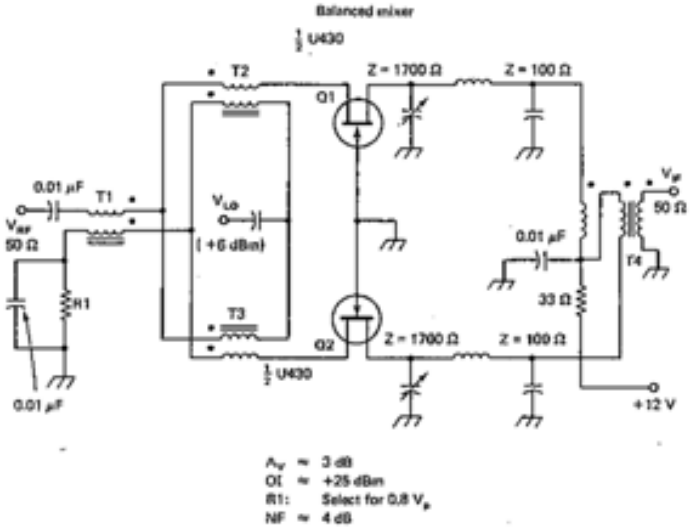


Figure 6.7 Dual FET balanced mixer using a Siliconix U430 device.

Figure 3.2: DeMaw's Fig. 6.7.

§9 I understand that in the ParkerVision v. Qualcomm trial, there were arguments regarding the invalidity of claim 18 of the '342 patent in view of a circuit disclosed in a text book by DeMaw, which is similar to the circuit from Oxner. The circuit from DeMaw (Ex. 1016) is reproduced here as Fig. 3.2.

§10 Claim 18 requires "performing a plurality of charging and discharging cycles of the first and second capacitors to generate first and second downconverted information signals across first and second impedance devices, respectively." (Ex. 1001 52:49-52.) In post-trial motions the patentee argued that DeMaw did not disclose this element since Qualcomm's expert had admitted that the downconverted signals were first observable immediately after the switches (Q1 and Q2) and before the impedance devices. (Ex. 1017: D.I. 516 at 13.) In particular, the patentee argued as follows: "Dr. Razavi testified that the first and second downconverted information signals in DeMaw are observed immediately after the switches in Figure 6-7 before the impedance devices (Trial Tr. 10/11 at 156:15-158:14, 164:15-18, 253:4-8, 259:8-12, 260:7-19). Because Dr. Razavi's opinion is that the downconverted information signals are generated *before* the impedance devices, the signals disclosed in DeMaw cannot satisfy the limitation that the first and second downconverted information signals are generated across first and second impedance devices." (Id., emphasis in original.)

§11 I disagree with patentee's interpretation of claim 18.

§12 The figure in DeMaw is similar to FIG. 16H of the '342 patent (reproduced here as Fig. 3.3) in that it has the switches positioned upstream of the capacitors and impedance

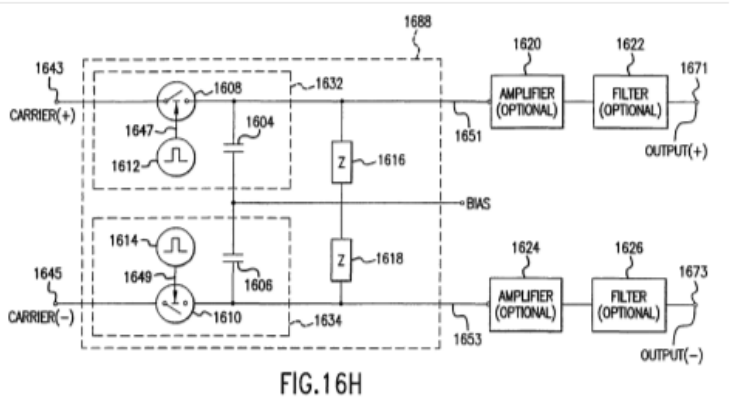


Figure 3.3: FIG. 16H in the '342 patent.

devices. Figure 16H is described in the '342 specification as performing this claimed step. (Ex. 1001 49:30-34; FIG. 62.) As explained below, in FIG. 16H, as well as in the capacitor-first arrangement of FIG. 16A, the downconverted signals are observable immediately after the switches and before the impedance devices. Accordingly, patentee's implied limitation that the downconverted signals cannot be observable before the impedance devices would exclude the preferred embodiments described in the patent's specification.

§13 First, in Figure 16H, the switches 1608 and 1610 are the *only* devices that can perform frequency translation, because they create a periodically time-varying branch in the circuit. The capacitors 1604 and 1606 and the impedance devices 1616 and 1618 are *linear, time-invariant* elements that *cannot* translate frequency. Frequency translation requires a periodically-operated switch or a non-linear device[3]. This is recognized in both the '342 specification (Ex. 1001 FIG. 1B, 6:10-11 ("The UFT modules perform frequency translation operations.") and one of the provisional applications listed on the face of the '342 patent.; Ex. 1011 70 ("Hundreds of authors have established that any harmonic function combined with a switch or other non-linear device can both up convert and down convert, preserving the information content bilaterally.").) This must also apply to Figure 16A.

§14 Second, in both FIG. 16A and 16H the downconverted signal exists as a voltage on a wire, extending from the output of the switch to the input of the optional amplifier in FIG. 16H and from right plate of the capacitor to the optional amplifier in FIG. 16A. It is a fundamental axiom of electrical engineering that the voltage with respect to any datum must be the same everywhere on a perfectly conducting wire. Accordingly, in all of the embodiments in the specification any downconverted signal across the impedance device would necessarily be observable up-stream.

[3]This is, of course, very well-established in electrical engineering. For example, a classic textbook [9, Sec. 8.2] lists four methods of frequency translation, of which two are: periodic switching, referred to as "chopper modulation"; and "nonlinear device modulation".

§15 In my view, a person of ordinary skill in the art would not have understood the "generate" element of claim 18 in the way suggested by the patentee in its post-trial motions. Instead, one of ordinary skill would have understood that to generate the downconverted signals across the impedance devices would mean to cause the downconverted signal to exist across those devices, recognizing that the frequency translation is effected by the periodically-operated switch alone.

> **Claim 342-19.** *The method of claim 18, wherein the first capacitor discharges between six percent to fifty percent of the total charge stored therein during a period of time that the first switching device is open, and wherein the second capacitor discharges between six percent to fifty percent of the total charge stored therein during a period of time that the second switching device is open.*

While the switch is open, a capacitor C will discharge into a resistance R that is connected across it. Over a switch-open time of T_{off}, the fractional discharge $\Delta Q/Q$ is given by

$$\frac{\Delta Q}{Q} = \exp\left(-\frac{T_{off}}{RC}\right) \tag{3.1}$$

From this expression it follows that for the charge to decay by 6%—that is to 94% of its original value—$T_{off} = 0.06 \times RC$. For it to discharge by 50%, $T_{off} = 0.69 \times RC$. Therefore, any T_{off} that lies in this range will satisfy the claim.

3.5 Prior Art: ParkerVision '551 Patent

By obvious extension to a differential realization (see Sec. 3.3 above), the embodiment described in ParkerVision's earlier '551 patent (67: 22-25), $T_{off} = 9.45\,\text{ns}$ and $RC = 2\,\text{k}\Omega \times 18\,\text{pF} = 36\,\text{ns}$. In this case $T_{off} = 0.26 \times RC$, which lies in this range. The earlier patent satisfies the limitation recited by this claim.

3.6 Prior Art: Estabrook (1989)

By obvious extension to a differential embodiment, [8, Fig. 14] shows the method of Claim 18 where $T_{off} = 0.55\,\text{ns}$ and $RC = R_L C_{LD} = 2.8\,\text{ns}$. Thus $T_{off} = 0.19 \times RC$, which satisfies the limitation of this claim.

The circuit of [8, Fig. 79] may be extended to a differential embodiment (with differential output) following the transformation of Fig. 4.20(a) into Fig. 4.20(d) found in [6]. The differential embodiment thus obtained, now with two capacitors loaded by two resistors, shows the method of Claim 18. $T_{off} = 0.55\,\text{ns}$ in this circuit, and $RC = R_L C_{LD} = 5.6\,\text{ns}$. Since $T_{off} = 0.09 \times RC$, this satisfies the limitation of this claim.

Claim 342-20. *The method of claim 18, wherein the first capacitor discharges between ten percent to twenty-five percent of the total charge stored therein during a period of time that the first switching device is open, and wherein the second capacitor discharges between ten percent to twenty-five percent of the total charge stored therein during a period of time that the second switching device is open.*

Applying (3.1) to the terms of this claim, T_{off} must lie in the range of $0.1 \times RC$ to $0.29 \times RC$.

3.7 Prior Art: ParkerVision '551 Patent

By obvious extension to a differential realization, the preferred embodiment in ParkerVision's earlier '551 patent (67: 22-25), with $T_{off} = 0.26 \times RC$, lies in this range.

3.8 Prior Art: Estabrook (1989)

By obvious extension to a differential embodiment (see Sec. 3.3 above), [8, Fig. 14] shows the method of Claim 18 where $T_{off} = 0.55\,\text{ns}$ and $RC = R_L C_{LD} = 2.8\,\text{ns}$. Thus $T_{off} = 0.2 \times RC$, which satisfies the limitation of this claim.

Claim 342-21. *The method of claim 18, wherein the first capacitor discharges between fifteen percent to thirty percent of the total charge stored therein during a period of time that the first switching device is open, and wherein the second capacitor discharges between fifteen percent to thirty percent of the total charge stored therein during a period of time that the second switching device is open.*

Applying (3.1) to the terms of this claim, T_{off} must lie in the range of $0.16 \times RC$ to $0.36 \times RC$.

3.9 Prior Art: ParkerVision '551 Patent

By obvious extension to a differential realization, the embodiment described in ParkerVision's earlier '551 patent (67: 22-25), with $T_{off} = 0.26 \times RC$, lies in this range.

3.10 Prior Art: Estabrook (1989)

By obvious extension to a differential embodiment (see Sec. 3.3 above), [8, Fig. 14] shows the method of Claim 18 where $T_{off} = 0.55\,\text{ns}$ and $RC = R_L C_{LD} = 2.8\,\text{ns}$. Thus $T_{off} = 0.2 \times RC$, which satisfies the limitation of this claim.

3.11 Commentary on Claims 19, 20, 21

§16 Discharging the sampling capacitor C through the resistor R during the switch OFF time T_{off} shows no benefit to the noise figure of the downconversion mixer. This discharge only lowers the mixer's gain, which means that the noise of subsequent stages in the receiver will contribute more significantly to the receiver's overall (cascade) noise figure.

Furthermore, with too large a leakage per sampling cycle, the mixer's own noise figure deteriorates.

§17 Therefore, while the sections above show that there is prior art to Claims 19, 20, and 21, I see no practical merit in these claims towards building a better downconversion mixer. Indeed they lead away from a good design, which requires leakage or discharge to be minimized.

Claim 342-23. *The method of claim 18, further comprising the step of: removing a carrier signal from the first and second downconverted information signals.*

3.12 Prior Art: ParkerVision '551 Patent

We extend the receiver described in ParkerVision's earlier '551 patent (67:22-25) by obviousness to satisfy the differential realization of Claim 18. The "Storage Capacitance" C and the $R_S = 50\,\Omega$ source resistance of the "Input EM Signal" form a lowpass filter with a cutoff frequency of $1/(2\pi R_S C) = 177\,\text{MHz}$. Irrespective of the ON time of the switch, this filter attenuates the 900 MHz carrier signal by at least 14 dB. Therefore, this embodiment taken from ParkerVision's earlier patent satisfies the subject claim.

3.13 Prior Art: Oxner (1979)

In [1, Fig. 2] (reproduced in Fig. 3.1(a)) the downconverted information signals appear across sampling capacitors C6 and C8. These capacitors are connected to inductors L1, L2 and capacitors C7, C9 to form a pi-network lowpass filter with a resonant frequency of roughly $1/(2\pi\sqrt{L1 \times C6 \parallel C7})$ Hz. In this embodiment, this cutoff frequency is 30 MHz while the LO frequency is 120 MHz. Since the filter is essentially second-order, it attenuates the RF and LO signal in the first and second downconverted outputs by a factor of about $4^2 = 16$, or 24 dB.

Fig. 3.1(b) shows the simulated voltage waveforms across C6 and C8. The carrier wave is clearly attenuated at the filter output.

3.14 Prior Art: Estabrook (1989)

We extend Estabrook's receiver by obviousness to satisfy the differential realization of Claim 18. The receiver operates by superposing a large current at the LO frequency (I_{LO}) on a small

RF current (I_{RF}). One half cycle of I_{LO} will forward bias the diode which then provides a bidirectional current flow path for the small I_{RF}, in just the same way as an FET switch would. The diode switching action shifts the RF current to an IF. The current through the diode is filtered by the first-order lowpass filter defined by the time constant $R_L C_{LD}$. Using the values for this time constant given in Sec. 3.8, the cutoff frequency is 57 MHz or less. This will pass an IF up to the cutoff frequency with negligible attenuation, but attenuate the RF and LO frequency of 900 MHz by 24 dB or more.

References

[1] E. Oxner, "FETs in Balanced Mixers," Siliconix, Application Note AN 72-1, 1979, (Ex. 1004).

[2] "U430/431 Matched N-Channel JFET Pairs," Siliconix, Data Sheet P-37405—Rev.D, 1994, (Ex. 1023).

[3] S. A. Schelkunoff and H. T. Friis, *Antennas: Theory and Practice*. New York: Wiley, 1952, (Ex. 1024).

[4] R. D. Thornton, C. L. Searle, D. O. Pederson, R. B. Adler, and E. J. Angelo, Jr., *Multistage Transistor Circuits*. New York: Wiley, 1965, (Ex. 1008).

[5] K. Bult and H. Wallinga, "A CMOS Four-Quadrant Analog Multiplier," *IEEE J. of Solid-State Circuits*, vol. 21, no. 3, pp. 430–435, Jun 1986, (Ex. 1009).

[6] H. J. Zimmerman and S. J. Mason, *Electronic Circuit Theory*. New York: Wiley, 1959, (Ex. 1020).

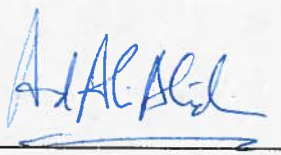
[7] H. E. Jones, "Dual output synchronous detector utilizing transistorized differential amplifiers," U.S. Patent 3,241,078, March 15, 1966, (Ex. 1021).

[8] P. Estabrook, "The Direct Conversion Receiver: Analysis and Design of the Front-End Components," Ph.D. dissertation, Stanford University, 1989, (Ex. 1006).

[9] K. K. Clarke and D. T. Hess, *Communication Circuits: Analysis and Design*. Reading, MA: Addison-Wesley, 1971, (Ex. 1026).

1. In signing this declaration, I understand that the declaration will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I acknowledge that I may be subject to cross examination in the case and that cross examination will take place within the United States. If cross examination is required of me, I will appear for cross examination within the United States during the time allotted for cross examination.

2. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the results of these proceedings.



July 2, 2014

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Date