

# Using an IQ Data to RF Power Transmitter to Realize a Highly-Efficient Transmit Chain for Current and Next-Generation Mobile Handsets

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**Abstract**— Combining and re-organizing the functions of multiple traditional transmitters and power amplifiers into a single unified multi-mode non-linear system results in improved performance and high efficiency. This in turn decreases the transmit chain footprint and lowers the bill of materials for applications such as mobile voice, data terminals, and femtocells. With this approach, RF designers will no longer be forced to choose between performance and efficiency, or reliability and cost, freeing them to design more optimal wireless systems.

## I. INTRODUCTION

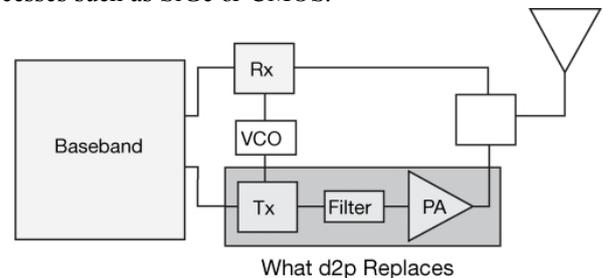
The continuing evolution of wireless communication standards and the associated increases in functionality in mobile wireless voice and data devices are driving an increasing demand for transmitters and power amplifiers that offer increased performance and flexibility while simultaneously consuming less power. For example, interleaving LTE channels within existing 900 and 1800 MHz spectrum is being discussed for the European Union, requiring mobile devices that can alternate between EDGE, UMTS and LTE. These new applications have more demanding size and cost requirements, and the next generation transmitters need to have a smaller footprint area and be implemented in common semiconductor technology.

As a result of the aforementioned design considerations, engineers struggle with trade-offs between power consumption, power output, linearity, and footprint area. In order to make progress towards the consumer and network provider's needs and expectations, designers have been utilizing increasing amounts of digital circuitry, which can be inherently smaller and more flexible than pure analog implementations. However, due to the fact that propagating radio waves is an analog process, the digital advantages at RF are limited.

Consequently, using traditional design approaches, the RF-transmit chain, particularly the power amplifier (PA), remains outside of the digital, system-on-a-chip (SoC) domain. Several manufacturers are offering standard-specific modulators and receivers that are integrated into the same package as the digital baseband processor but due to a host of different design considerations, the PA remains an external component. The questions for designers now become: How many PAs will be

required to support multi-standard, high-power phone applications? What type of efficiency can be achieved with the ever increasing peak to average power ratios of W-CDMA, CDMA2000, HSPA, LTE and WiMax?

A new approach to transmitter-PA design and functionality known as d2p™ is presented and discussed herein as an alternative to the traditional transmitter-PA circuitry. The d2p architecture combines and re-organizes the functions of a traditional transmitter and power amplifier into a single unified non-linear system. The result is a single set of circuitry that simultaneously aligns efficiency and linearity while offering unparalleled waveform flexibility. In addition, a d2p design reduces the footprint area of the transmit function and can be implemented in common semiconductor processes such as SiGe or CMOS.



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Fig. 1 d2p Input: Digital I/Q, d2p Output: Signal at Power

## II. OVERVIEW

A switch is the most efficient means of creating an amplified RF output. Switching amplifiers are non-linear by definition and can be designed to be more efficient than linear or pseudo-linear devices. The additional amplifier efficiency provides the required output power from a smaller device and reduces unwanted heat. However, in order to meet output waveform linearity requirements, a suitable control system and switching amplifier architecture must be chosen.

Traditional approaches to vector power-amplification (VPA) architectures allow switching amplifiers to operate on constant-envelope signals and reconstruct the modulation envelope at the output using outphasing control and combiners. This classical approach necessitates extreme outphasing

vector accuracy to create compliant waveforms and requires a power combiner which increases the size and cost of the implementation. By contrast, in a d2p system, optimal vector-power-amplifier performance is achieved using a variety of processing and control functions that act in concert and eliminate the need for extreme vector accuracy and the power combiner.

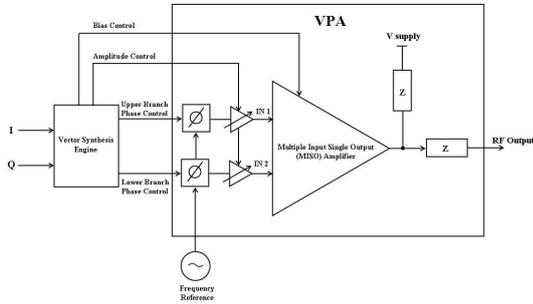


Fig. 2 d2p Block Diagram

This alternative transmitter system design shown in Fig. 2 is comprised of two primary blocks, the vector-power amplifier (VPA) and the vector synthesis engine (VSE). The VSE controls three VPA control functions, upper and lower branch phase control, amplitude control and bias control. As implemented the VSE is a digital state machine and uses approximately 250K gates.

Fig. 3 provides further contrast between d2p VPA operation and a traditional outphasing system.

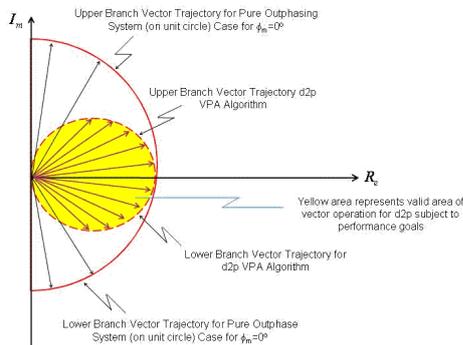


Fig. 3 d2p Multi-Control Function versus Outphasing Vector Generation

In a traditional outphasing system, the upper and lower branch vectors are constant amplitude and remain on the unit circle. In the d2p architecture, both the phase and amplitude of the upper and lower branch vectors are allowed to change.

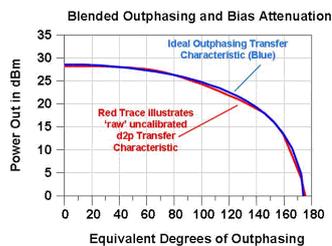


Fig. 4 d2p versus Outphasing Transfer Characteristic

Fig. 4 compares a perfect (no amplitude or phase errors over 180 degrees) outphasing transfer characteristic with an actual d2p transfer characteristic without calibration. The d2p multi-control transfer function also referred to as blended control is dynamically related to the signal modulation format and waveform statistics as shown in Fig. 5.

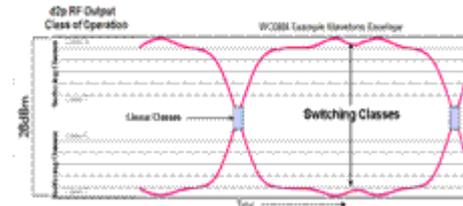


Fig. 5 d2p WCDMA Blended Control Example

Under the control of the VSE, the blended control function results in high non-linear amplifier efficiencies over the majority of the waveform trajectory. In order to eliminate the extreme vector accuracy requirements of a traditional outphasing system, the VSE transitions the d2p VPA branch amplifiers towards increasingly linear states as the waveform instantaneous power output requirements are reduced and starts to turn them off when approaching a zero crossing.

### III. DESIGN DETAILS

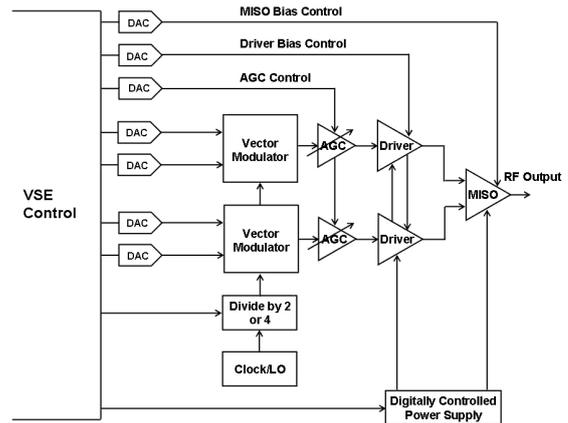


Fig. 6 d2p Architecture Detailed Block Diagram

Fig. 6 is a detailed block diagram that shows the functions and interconnectivity necessary for a d2p design. The VSE and DACs are currently implemented in 65nm CMOS and the VPA is implemented in both 0.18u and 0.13u SiGe.

A unique multiple-input-single-output (MISO) amplifier is employed to eliminate the classical combiner structures found in traditional designs. The MISO architecture enables a true monolithic implementation. The MISO is designed not to be two independent power amplifiers that must be balanced and isolated from each other as in traditional outphasing systems, but as a single output device with two or more inputs.

Fig. 7 is an exemplary MISO output simulation. At higher power outputs and an upper and lower phase difference of zero (0) degrees and proper bias levels, the output voltage and

current waveforms of the MISO approximates those of a class-E amplifier.

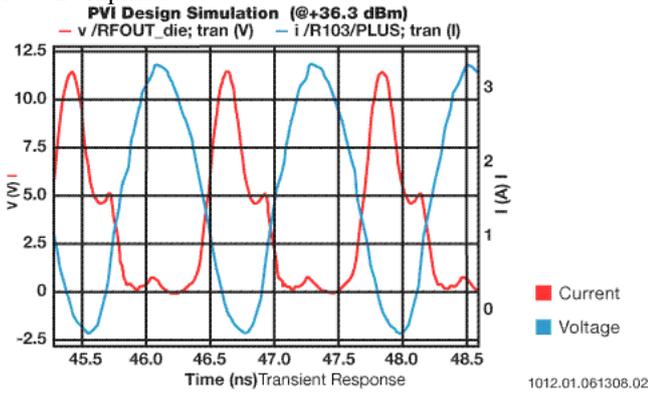


Fig. 7 Simulated MISO Output Voltage and Current at +36dBm Output

As the phase difference between the upper and lower branches varies as shown in Fig. 3, the MISO output approximates a class-S amplifier with the corresponding change in output duty cycle. For waveforms such as WCDMA, the d2p system operates in class-S mode over 92% of the time. As the WCDMA waveform envelope starts towards a zero crossing, the blended control function will force the MISO amplifier through different conduction angles and therefore different classes of amplification. It is important to observe in Fig. 5 that the d2p system remains in a non-linear, highly efficient operation class mode over 97% of the time for a WCDMA waveform. By manipulating a variety of conditions within the VPA branches, the d2p blended control functions vary the operational class of the MISO amplifier and dynamically impose regions of operation that vary between saturation and cut off as a function of waveform envelope and associated waveform statistics.

For the current implementation, Fig. 8 represents a MISO conceptual schematic.

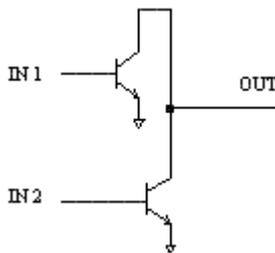


Fig. 8 MISO Conceptual Schematic

The upper and lower branch vector modulators use internally referenced In-phase and Quadrature signals that are derived from the Clock/LO source to produce on-frequency phase varying constant envelope signals with a variable outphasing offset. The original I and Q information from the baseband source is decomposed by the VSE and used to derive the vector modulator inputs.

Coupled together, the AGC circuitry and the Digitally Controlled Power supply achieve greater than 85dB of power output control monolithically, without using an attenuator. The d2p AGC and Digitally Controlled Power Supply

bandwidth is equal to the cellular system automatic gain control update rate of the supported standards which varies from 80Hz to 1500Hz. This is in sharp contrast to a polar system that requires the switching power supply to have multiple times the bandwidth of the output waveform as well as precise synchronization with the phase modulation.

The Driver circuitry ensures that the MISO can achieve the required output power for a given application. The Driver circuitry can be considered an extension of the MISO amplifier and thus can share its control functions.

#### IV. VECTOR SYNTHESIS ENGINE

The VSE is a small, low-power digital state machine that accepts traditional synchronous baseband I-Q information and performs a variety of algorithmic functions including coordinates system transformations for complex signal representation, vector transforms and associated translations, d2p system characteristic transfer function generator, and an optimized VPA blended control algorithm. The VSE to VPA analog input interface is implemented through D/A functions and simple reconstruction filters.

#### V. PERFORMANCE

Two models, a low-band (824-915 MHz) and a high band (1710-1980 MHz) have been designed, produced and tested, using the 180 nm and 130 nm SiGe processes available from IBM. The 180 nm low-band VPA IC is shown in Fig. 9 below. As shown, the complete VPA IC includes LO dividers and complementary vector modulators, AGC amplifiers, Drivers, and the MISO amplifier. All data was taken on single samples of the device for the respective high band or low band. The devices are capable of very high efficiency across a broad range of power output levels and signaling waveforms, as exemplified in Fig. 14.

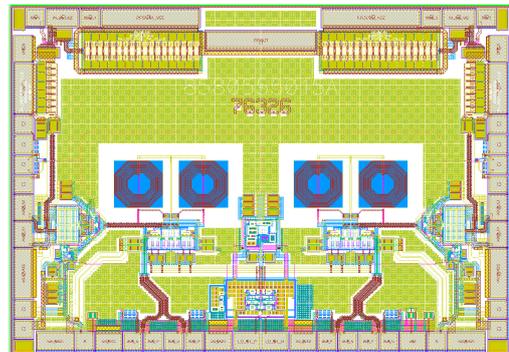


Fig. 9 Low-Band VPA IC in 180nm SiGe

For the purposes of this paper, waveforms of a variety of modulation types were taken from the same design of high-band device. A single design is capable of producing high modulation accuracy for a host of different waveforms as shown in Figs. 10-11. The selected waveforms are: LTE, EDGE, WCDMA, and HSUPA.

The d2p designs also possess exceptional frequency and temperature performance. Power output over 80dB of

dynamic range and ACPR/ACLR are well behaved over all operational parameters as shown in Figs. 12-13.

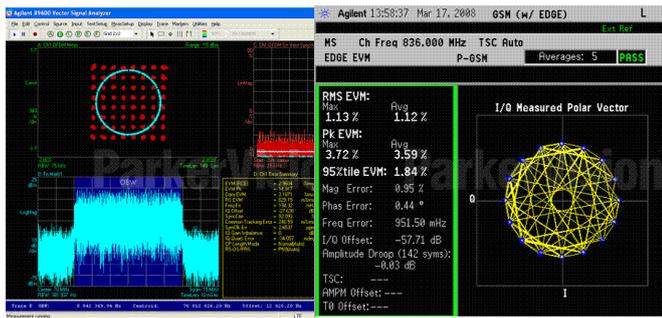


Fig. 10 LTE and EDGE Mod. Accuracy

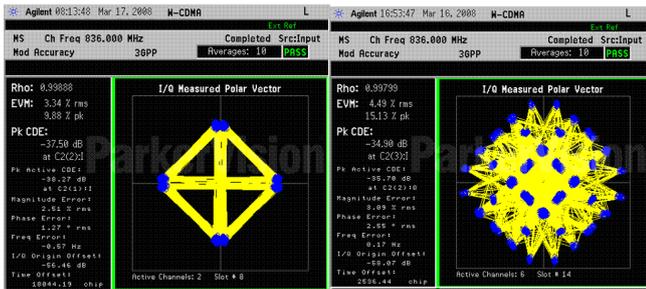


Fig. 11 WCDMA and HSUPA Mod. Accuracy

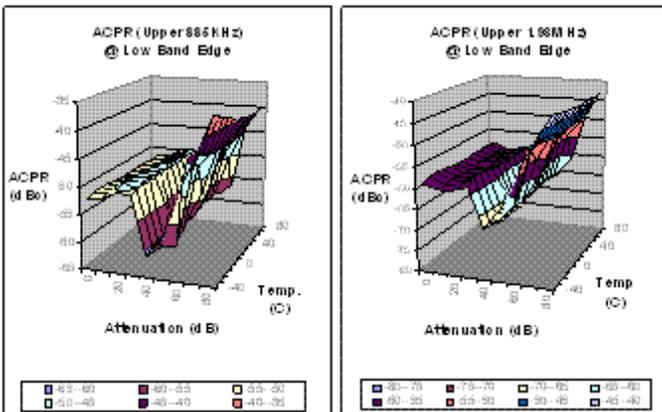


Fig. 12. Upper 885kHz and 1.98MHz ACPRs @ Low Band Edge

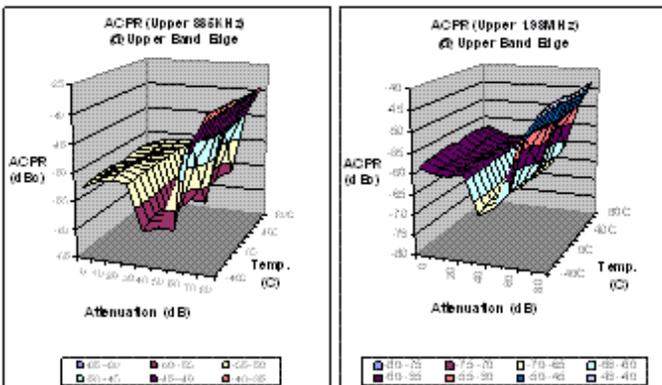


Fig. 13 Upper 885kHz and 1.98MHz ACPRs @ Upper Band Edge

The utilization of non-linear amplification makes the d2p architecture efficient for both constant envelope and high peak-to-average-power ratio (PAPR) waveforms. For purposes of illustration, a WCDMA 1\_1 waveform efficiency is shown in Fig. 14 for the Driver/MISO, the complete VPA IC, and the complete d2p system including the VPA, the VSE and baseband interface (Digital I/Q Baseband to RF Power Output). In addition, the complete d2p system total current in milliamps normalized to 3.6 Volts is shown in Fig. 15.

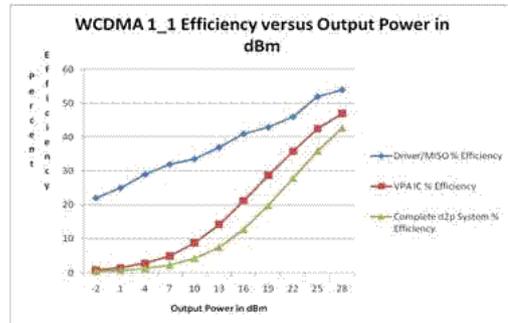


Fig. 14 WCDMA Efficiency versus Output Power

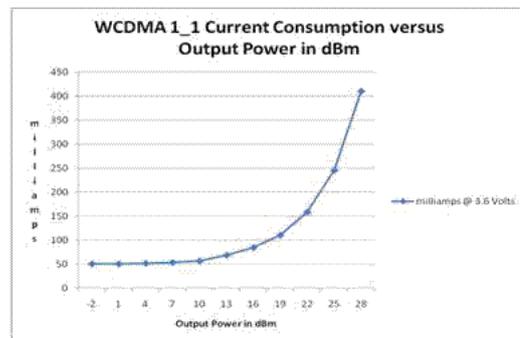


Fig. 15 Current Consumption in milliamps versus Output Power

## VI. CONCLUSION

When implementing d2p technology, RF designers will no longer be forced to choose between performance and efficiency, or reliability and cost. The d2p architecture represents a significant increase in talk time along with a reduction in the size and cost of the phone. This new design technique enables device manufacturers to replace multiple transmit chains from their multi-mode designs with a single d2p implementation and natively support multiple network standards without additional transmitters and power amplifiers. This, in turn, decreases the transmit chain footprint, lowers the overall bill of materials cost, and increases design reliability.

## REFERENCES

- [1] S. C. Cripps, *Advanced Techniques in RF Power Amplifier Design*, Artech House, Inc., 2002.
- [2] F. H. Raab, P. Asbeck, S. Cripps, P. B. Kenington, Z. B. Popovic, N. Pothecary, J. F. Sevic, and N. O. Sokal, "RF and Microwave Power Amplifier and Transmitter Technologies-Part 1-5," *High Frequency Electronics*, May 2003, September 2003, November 2003, January 2004.